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To Study of GAN Based Primary Double Gate Junctionless Tunnel FET: A Review

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***Abstract*— In this paper explores the performance of GaN based double gate n-channel junction less tunnel FET (JL-TFET) and its comparatively new technology, which is suitable for low power applications. To overcome the major challenges faced by conventional MOSFET and it reduces the low current driving capability, ambipolar behavior of the TFET. In this material enhances the device performance especifically the faster switching, compact size, low ON resistance, less capacitance improved thermal conductivity and relatively lower cost than Si devices. In JLTFET select the appropriate work function and interfaces is to improve the ON current and ambipolarity. In this optimization to provide idea to select the appropriate length direction towards the practical feasibility at the experimental level values tried to achieve in this.**

***Index Terms*— DoubleGate,Ambipolar nature, Junction less TunnelFET (JL-TFET), steepsubthreshold slope,sentaurus TCAD simulator..**

I. INTRODUCTION

A MOSFET's size scales down, the low power dissipation in the circuit is maintained by reduced supply voltage. The electrical parameters such as Sub threshold Swing (SS) and threshold voltage (VT) should be very less. But the SS is limited to 60 mV/decade in MOSFETs1and to reduce the low current driving capability (due to limited amount of charge carriers tunneling through the junction) and ambipolar behavior (conduction for both positive and negative edges). To overcome this, several novel devices with various transport mechanism have been reported. In JL- TFET particularly used for the device in low power applications in terms of power efficiency, fabrication complexity and size.

On the other hand, compound materials like GaAs, SiC and GaN have been tried and tested for high power and high frequency application because of their unique properties. The material enhances the device performance such that faster switching, compact size, High ON current, low resistance, improved thermal conductivity and reliability with lower cost than Si devices. The viability of a material for high frequency and high power can be measured by using this formula Johnson figure of merit (JFOM) and Baliga figure.

we have explored a new technique to form JL-TFET, where first P+substrate is considered in the GaN body and then metal electrodes with specific

Work functions are applied to form the channel and drain regions. This removes the barrier present between source and gate electrode of conventional JL-TFET, which improves the ON-current of the device. GaN based junction less tunnel FET reveled to have high driving current capability, low leakage current, ideal subthreshold behavior and reduced the temperature sensitivity due to the excellent gate electrostatic control over the narrow channel. In this junction less tunnel FET have been analyzed by incorporating the device in the design of inverter and peculiar advantages for the circuit design based on its operational parameters are analyzed. In recently, Dong Ji et al. have been demonstrated a GaN n-channel JFET which can provide normally OFF operation and another well-suited device than GaN HEMTs for power applications with breakdown voltage and ON resistance approximately 1260 V and 5.2 mΩ cm2, respectively. Due to the high breakdown field strength, GaN n-channel JFET like the other GaN material-based devices with vertical geometry can sustain very high-operating voltages across it. Therefore, integrating the advantages of the junction less technology for reducing fabrication complexity, GaN material for its excellent properties and vertical geometry for obtaining high current density and high breakdown voltage are the motivations in proposing the GaN n-channel JLFET for power applications.

II. DEVICE DESCRIPTION, SIMULATION, AND FABRICATION

The sentaurus TCAD simulator (synopsis) is used for this investigation. This figure shows the schematic and simulated structure of the junction less tunnel FET. Simulation along with length and thickness of different layers used. In this simulation includes the effect of high and normal electric field in the velocity saturation. Band to Band tunneling has been used along with Fermi-statics. In high impurity atom in the channel Shockley-Read-Hall (SRH) model can be included.

In this simulation band structure of the junction less tunnel FET shows the OFF and ON states. Electrons tunneling through the junction easily and source –channel region tunneling barrier Width is lowered during this ON state.

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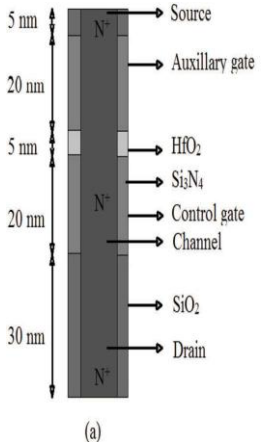

Figure 1. Schematic structure of the JLTFET

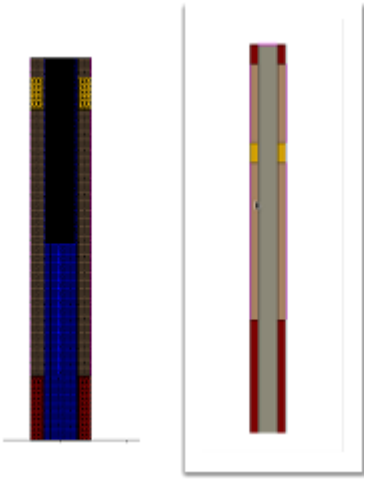

Figure 2. GaN based structure of the JLTFET

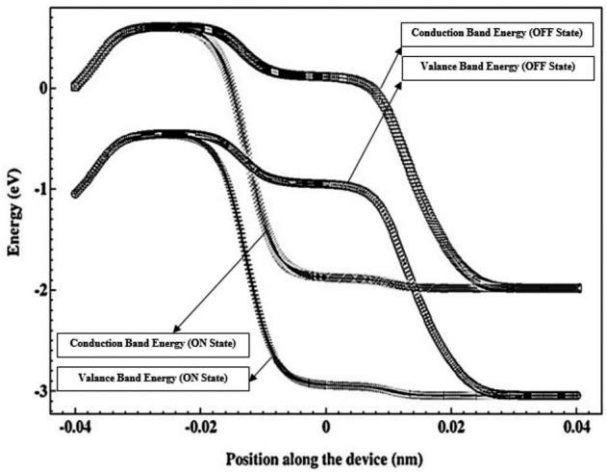

Figure 3. Band structure of Junction less tunnel FET

Schematic of the documented device (VC-JFET), + having the aperture length (Lap) and drift region capable zero.9 and eleven µm, severally, with n-GaN doping concentration of 1016 cm3 and

P-GaN cur- rent blocking layer (CBL) doping concentration of the order of 1019 cm3

The absence of any p–n junction reduces traps and defects in the process of device fabrication. It also reduces the fabrication complexity and cost as no p-GaN or extra regrowth of material is required. The aperture region of the proposed device is formed by depletion of electrons from both sides of the device due to the work-function difference of gate and n-GaN materials.

The gate and drain voltages controlled the flow of electrons. Below the gate at Zero bias. It is a newer technology as compared to Si obtaining good quality free standing GaN substrate is a complex and costly affair. Therefore, the affordable methods discovered for obtaining GaN substrate, other materials like Sapphire, SiC, and Si substrate are used as a substitute for GaN substrate, but have their construction.

For example, Sapphire cost is less, but heating problem occurs due to poor thermal conductivity.

Si substrates are less costly due to being a well-established technology and have better thermal conductivity as compared to sapphire substrates.

Therefore, the Si substrate solve heating additionally as price issue up tgood extent, but have lattice mismatch related problems with GaN. In spite of the aforesaid complications, Si is used as a substrate for growing GaN with important results.

Recently, a 6-inch diameter GaN wafer on Si substrates has been reported which could be enough to be used in production.

Electrical Properties of GaN

properties	Si	GaAs	SIC	InP	GaN
Electron Mobility	1400	10000	800	5400	2000
E-band gap(Eg)	1.12	1.4	3.26	1.34	3.4
Ebr-breakdownfield	0.3	0.4	3.5	0.5	3.3
Vsat-(saturation velocity)	1.0	1.5	2	0.67	2.5
n-density	<1	-1*	-	3*	15*
JFOM	1.0	9.6	3.1	22.3	24.6
BFOM	300	300	600	300	700

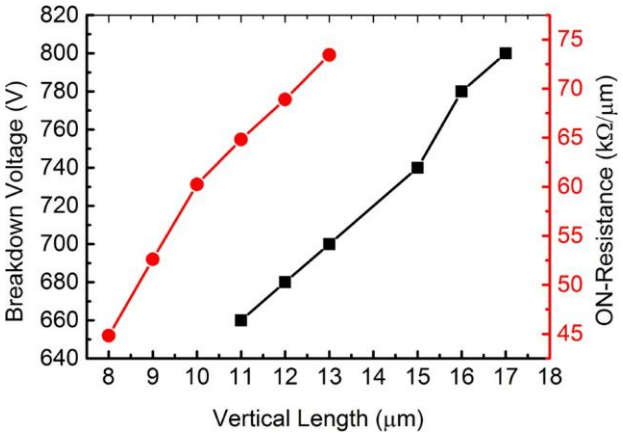

Figure 4: characteristics of break down voltage

III. Simulation Methodology

We have to perform the simulation using sentaurus TCAD software tool and various methods can be involved can be explained. A device simulation is taken as finite element structure. All node having special characteristics such as material type, doping concentration, current densities, electric field generation and recombination rates and many other parameters can be calculated using in this simulation.

Threshold Voltage (V_T) and subthreshold voltage (SS) are extracted using DC simulations and R_0, g_m and f_t. Calculated using AC simulations. From the I_d-V_g characteristics V_T is extracted which is the minimum voltage required to set up a current between source and drain. V_T is extracted by constant current method with

Threshold current of 10^{-7}A/µm. This is the method where in the gate voltage is extracted at which the drain current exceeds a given current level. SS is the amount of gate voltage required to establish a logarithmic change in the drain current.

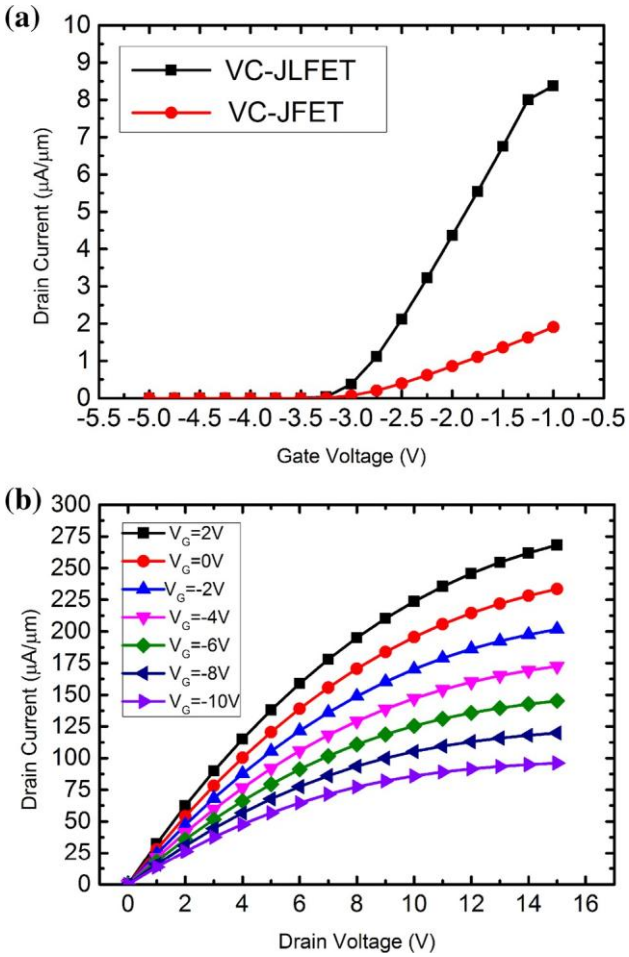

Figure 5: Id and Vg characteristics of current

IV. Conclusion

In this paper combines the working principle of JLFET and TFET. Analysis is used to calculate the Subthreshold Swing (SS), Threshold voltage (VT), intrinsic gain (gm) and Ft parameters are calculated. Subthreshold swing can be reduced Intrinsic gain can be increased in this analysis. To calculate High Ion/Ioff ratio of 5.8 × 1011 the value of can be calculated as 721.3GHZ and to promising the device can be suitable for RF frequency near in future. GaN resonant systems can be used for a variety of physical, chemical, and bio sensing applications.

References

[1] Ghosh, B., and M. W. Akram. 2013. "Junction less Tunnel Field Effect Transistor." IEEE Electron Device Letters 34 (5): 584–586

[2] Colinge, J.-P., C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, et al. 2010. "Nanowire Transistors without Junctions". Nature Publishing Group.

[3] Roop Narayanan Goswami, S. Poorvasha and Lakshmi.B "Tunable work function in junction less tunnel FETs for performance Enhancement." International Australian journal of Electrical and electronics engineering.

[4] Sukeshni Trikey, Dheeraj Sharma, Dharmendra Singh Yadhav, and Shivendra Yadav "Analysis of Novel Metal Implant Junctionless Tunnel FET For Better DC and Analog/RF Electrostatic Parameters' IEEE Transaction ON Electronic Devices VOL 64, NO.9

[5] Ball Mukund Tripathi.Shyama Prasad Das "Performance Evaluation of Normally ON/OFF Junction less channel GaN FET" Applied Physics A Material Science Enggineering in 2018

[6] Sunny Anand. S.Intekhahb Amin. R.K. Sarin "Analog Performance Investigation of Dual Electrode Based Doping Less Tunnel FET" J Computer Electron in 2018

[7] 7. T. Jaspar Vinithasundari, K. Karthika "Inverter Design Using Junction less GAA Tunnel Field Effect Transistor" International Journal of innvoatic Technology

[8] Fayzalloah Khorramrouz; seyed Ali sedigh Ziabari; Ali Heydari "Analysis and study of geometrical study of junction less Tunnel FET" Nano Dimensions 2018

[9] Mayryam Abedini.Seyed Ali sedigh Zibari.Abdollah Eskandarian "Representation of Hetero Structure electrically Doped Nano scale Tunnel FET with Gaussian-doping Profile for High- Performance Low-Power Applications" International Journal of Nano letters in 2018