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Study and Simulation of an Analogical-to-Digital Converter 8 Bits

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***Abstract*- According to the advantages of the digital signal processing, we turn us towards the numerical field. The design of digital circuits in the majority of cases is much less complex than its analogical counterpart. It is an incomparable flexibility and entrains a reduction of cost. The digital signal is stable, robust and insensitive to noise. It allows us to reach a very high degree of accuracy. However, the sources of the electrical signals are mostly analogical; consequently, these signals must be digitized for being treated numerically. The analogical-to-digital converters (ADC) constitute the bridge between the two fields (analogical and digital). The portable biomedical applications for instance have contributed to the development of more powerful analog-to-digital converters with a low consumption of energy compared to the speed of operation. The industrial development of the integrated circuits during the last decade was so fast, that it is now possible to integrate a complex system on just one chip. This evolution towards increasingly high levels of integration is justified by the needs for more powerful, light and compact systems with a minimum consuming power.**

In this paper, we design and simulate an analogical-to-digital converter. The digitalization of systems allows us less consumption of energy and higher precision. The principal architectures of analog-to-digital conversion are classified in two families: ADC at Nyquist rate (Nyquist rate converter) for those converters, the sampling rate (F_S) coincides with the Nyquist rate **of the ADC.**

These converters can be under various architectures like integrator, reallocation of burden-sharing, algorithmic, parallel Flash and pipeline. The ADC with oversampling, are the Sigma-Delta and the Sigma-Delta pass-band.

***Index Terms*—Digital signal processing, Analogical-to-digital converters, Digital-to- analogical converters, Simulation.**

I. INTRODUCTION

According to the advantages of the digital signal processing, we turn us towards the numerical field. The design of digital circuits in the majority of cases is much less complex than its analogical counterpart. It is an incomparable flexibility and entrains a reduction of cost. The digital signal is stable, robust and insensitive to noise. It allows us to reach a very high degree of accuracy. However, the sources of the electrical signals are mostly analogical; consequently, these signals must be digitized for being treated numerically.

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In this paper, we design and simulate an analogical-to-digital converter. The digitalization of systems allows us less consumption of energy and higher precision. The principal architectures of analog-to-digital conversion are classified in two families: ADC at Nyquist rate (Nyquist rate converter) for those converters, the sampling rate (F_S) coincides with the Nyquist rate of the ADC.

$F_S = 2*F_{max}$, where F_{max} is the maximum frequency of the input signal.

These converters can be under various architectures like integrator, reallocation of burden-sharing, algorithmic, parallel Flash, and pipeline. The ADC with oversampling, are the Sigma-Delta and the Sigma-Delta pass-band.

We recall in the first chapter the general information on the signals through the classification of the signals and the Fourier's transform. In chapters two and three we study successively the three stages of conversion (sampling, quantification and coding) and the analogical-to -digital converters through parallel converter or FLASH. In the fourth chapter, we utilize ISIS software of proteus to visualize signals; using the integrated circuit ADC0804 8 bits. We will recall the symbol of the ADC, its principal characteristics, the stitching of the integrated circuit ADC0804 and the scheme for realization of clock in the ADC. Last chapter discusses about the advantages and applicability of analogical-to-digital converters and digital-to- analogical converters.

II. STRUCTURE OF PAPER

The work is subdivided in five chapters. The first chapter gives us the general information on the signals through the classification of the signals and the Fourier's transform. In the chapters two and three we study successively the stages of conversion, and the analogical-to -digital converters through parallel converter or FLASH. In the fourth chapter, we utilize ISIS software of proteus to visualize signals; using the integrated circuit ADC0804 8 bits**.** The last chapter discusses about the advantages and applicability of

analogical-to-digital converters and digital-to- analogical converters.

III GENERAL INFORMATION ON THE SIGNALS

A. Classification o f the Signals

The deterministic (or certain) signal as temporal evolution can be described perfectly by a mathematical model.
There are two types of deterministic signals: periodic and no periodic signals.

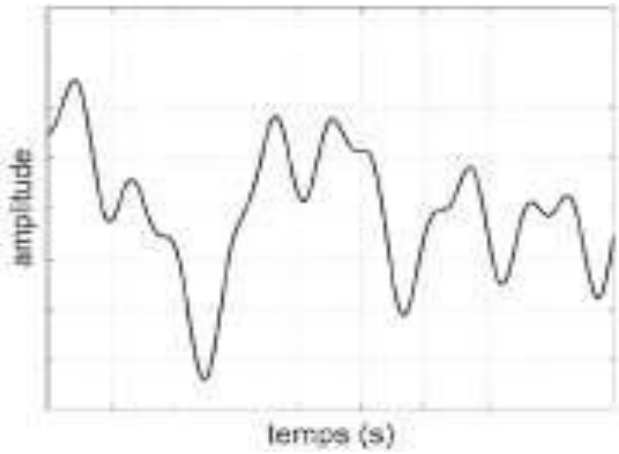


Figure -1: Deterministic signal

A signal s (t) is periodic of period T if it satisfies the relation: s (t) = s (t + T). We distinguish the sinusoidal signals, the pseudo-random signals (random signal which is repeated) and the periodic composite signals.

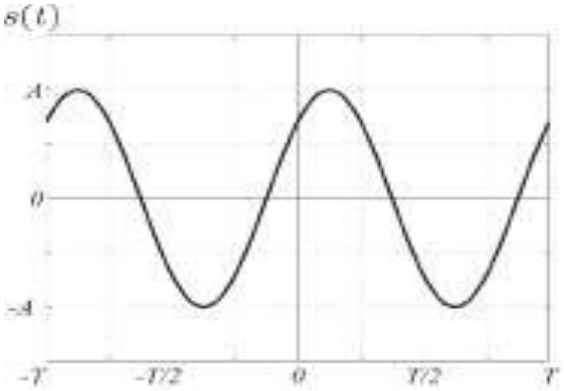


Figure- 2: Periodic signal

The no periodic signal does not satisfy the preceding relation. We distinguish the quasi-periodical signals which result from the sum of sinusoidal signals and the transitory signals (signals with limited duration).

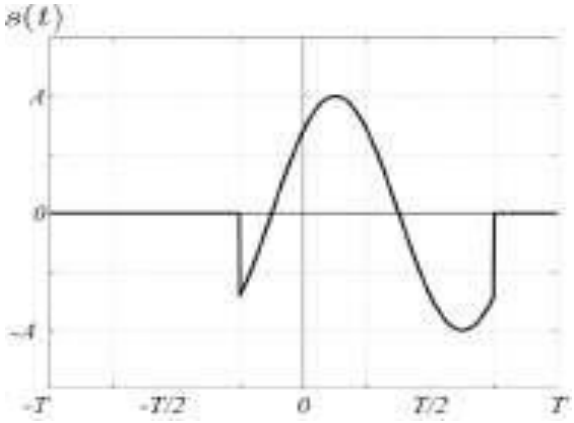


Figure -3: No periodic signal

The random, probabilistic or stochastic signal as temporal evolution is unforeseeable. It is characterized by statistical observations by using probabilistic tools. The majority of the signals are random because they are often disturbed or their position on the axis of times is unknown.

The random stationary signals whose statistical characteristics are invariants are no stationary. In practice, we consider that a signal is stationary throughout a finished observation.

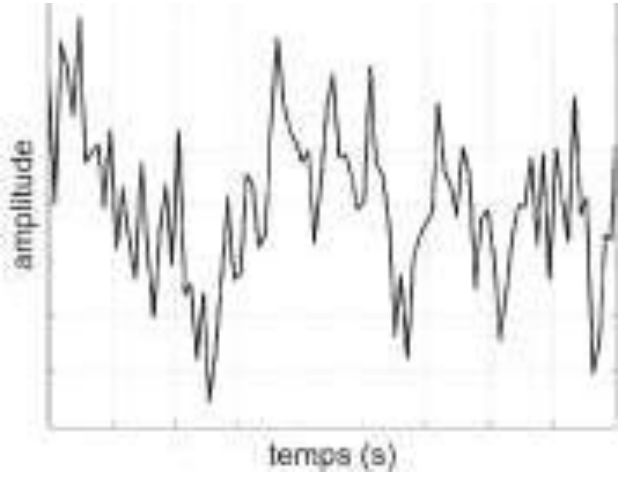


Figure -4: Random, probabilistic or stochastic signal

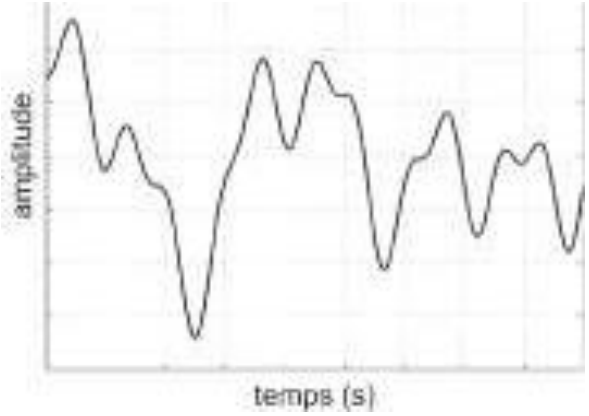


Figure -5: Signal with amplitude and time continuous

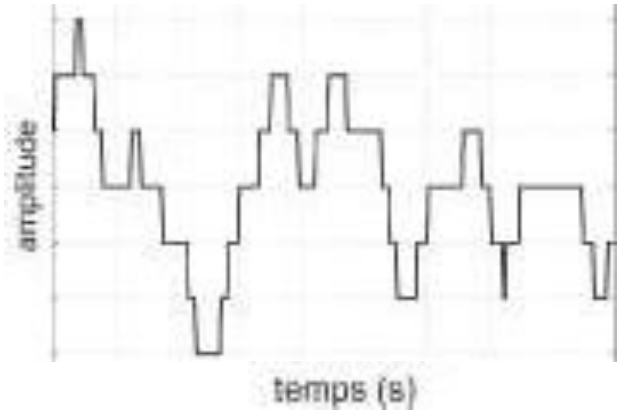


Figure-6: Signal with discrete amplitude and continuous time

The signal with continuous amplitude and discrete time (discrete signal): The values of the signal are available only at certain moments. These moments appear at the regular intervals,

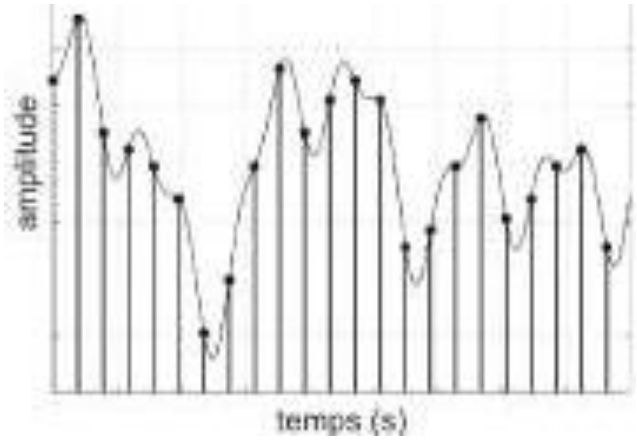


Figure- 7: Signal with continuous amplitude and discrete time (the signal is sampled).

B. Fourier Transform

The Fourier Transform is a generalization of Fourier series for any type of signals. To develop the Fourier transform, the principal idea is, to tighten the period T of a periodic signal towards the infinite. While inserting this condition in the Fourier series, we obtain the following relation according to the Fourier Transform of an aperiodic signal.

1) Fourier Transform of the periodic functions:

There are several types of Fourier Transform, according to the classes of analyzed signals or the type of generated signals: a Continue Transform for the signals at continuous time, a Continue Transform for the signals at discrete time, a Discrete Transform for the periodic signals at continuous time, the Discrete Transform of Fourier.

The continuous Fourier Transform of the signal x (t) of period T can be written:

$$x(t) = a_o + \sum_{k=1}^{+\infty} [a_n \cos(2\pi f_0 kt) + b_n \sin(2\pi f_0 kt)] \quad (1)$$

$$x(t) = a_o + \sum_{k=1}^{+\infty} \left[a_n \cos\left(\frac{2\pi}{T}kt\right) + b_n \sin\left(\frac{2\pi}{T}kt\right)\right] \quad (2)$$

With $f_o = 1/T$.

The coefficients a_k et b_k are given by:

$$a_k = \frac{1}{T}\int_{-T/2}^{+T/2} (xt)\cos(2\pi f_o t)dt$$

$$b_k = \frac{1}{T}\int_{-T/2}^{+T/2} (xt)\sin(2\pi f_o t)dt \quad (3)$$

Let us pose:

$X(kf_0)=(1/2)*(a_k - jb_k)$

$$x(t) = \frac{a_o}{2} + \sum_{k=-\infty}^{+\infty} X(kf_o)\exp(-j2\pi f_o t) \quad (4)$$

X (kf0) is the frequency spectrum, generally complex size, which can be decomposed into spectrum of amplitude and spectrum of phase:

$$|X(nk)| = \frac{1}{2}\sqrt{a_k^2 + b_k^2} \quad ; \text{ Spectrum of amplitude}$$

$$\varphi(kf_o) = arctg\left(-\frac{a_k}{b_k}\right) \quad ; \text{ Spectrum of phase} \quad (5)$$

From where

$$X(f) = TF[x(t)] = \sum_{k=-\infty}^{+\infty} X(nf_o)\exp(-j\varphi(kf_o)) \quad (6)$$

It is important to notice that the spectrum of a periodic function of period T is composed of lines whose minimum variation is fo = 1/T, on the axis of the frequencies. It's thus primarily discontinuous, it exists only for the values of the multiple frequency of fo ((n*fo), with n Є IN).

2) Fourier Transform of the no periodic functions:

The no periodic functions can be considered as an extension of the periodic function of the period T. The interval of frequencies fo = 1/T tends then towards zero and the spectrum then becomes a function which can be continuous.

In this case the TF of x (t) is by definition:

$$X(f) = \int_{-\infty}^{+\infty} (xt)\exp(-j2\pi ft)dt \quad (7)$$

We usually write: x(t) ⟷ X(f)

X (f) is a generally complex function

3) Fourier series as a cosine:

Taking into account the following trigonometrical relation:

$$A\cos(x) + B\sin(x) = \sqrt{A^2 + B^2}\cos\left(x + \arctan\left(\frac{-B}{A}\right)\right) \quad (8)$$

The development in Fourier series can be written:

$$x(t) = A_0 + \sum_{k=1}^{\infty} A_k \cos(2\pi k f t + \varphi_k) \quad (9)$$

With

$$A_0 = \frac{a_0}{2} \qquad A_k = \sqrt{a_k^2 + b_k^2}$$

$$\varphi_k = \arctan\left(\frac{-b_k}{a_k}\right) \quad (10)$$

This series is very important because it corresponds to the well-known description of the signals in permanent sinusoidal mode where the current (or the tension) is represented by its amplitude and its phase. From a practical point of view, x (t) is from an infinity of sinusoidal generators. Because of its spectral representation it's named unilateral spectrum.

4) Complex Fourier series:

Remembering the relations of Euler:

$$\cos(x) = \frac{1}{2}(\exp(+jx) + \exp(-jx))$$

$$\sin(x) = \frac{1}{2j}(\exp(+jx) - \exp(-jx)) \quad (11)$$

It is shown that the Fourier series can be transformed into a series of Complex Fourier.

$$x(t) = \sum_{k=-\infty}^{\infty} X(jk)\exp(j2\pi k f_0 t) \quad (12)$$

Coefficients X (jk) are complex:

$$X(jk) = \frac{1}{T}\int_{-\frac{T}{2}}^{+\frac{T}{2}} (xt)\exp(-j2\pi k f_0 t)\, dt$$

$$-\infty < k < +\infty \quad (13)$$

According to the graphic spectral representation, we call it bilateral spectrum. This description is analytically more interesting than the cosine form.

We note that the Euler formula replaces the functions sine and cosine by the exponential ones with imaginary exhibitor.

The development in Fourier series of a periodic signal x (t) can also be written in form:

$$x(t) = \frac{a_o}{2} + \sum_{k=1}^{\infty} A_x(k)\cos(2\pi f t + \varphi_x(k)) \quad (14)$$

With

$$A_x(k) = \sqrt{a_k^2 + b_k^2} \quad (15)$$

$$\varphi_x(k) = -\arctan\left(\frac{a_k}{b_k}\right)$$

$A_x(k)$ spectrum of amplitude

$\varphi_x(k)$ Spectrum of phase

IV. STAGES OF CONVERSION

The first phase of an analog-to-digital conversion is called sampling. This phase is carried out by the analog-to-digital converter. The samples are taken at the regular intervals of time by measurements series of the tension of the original analogical signal.

Sampled information allows reproduction more or less faithful of the analogical signal put at the input. More the number of measurements is important, more the duration between two measurements is small and thus more information will be contained in the digital signal. Then the digital signal will be more faithful to the original analogical signal.

More the number of measurements is important for a given time; more the sampling rate is high.

The digitalization of the signal is made in several phases: The hold of the value of the signal at the instant T (sampling); the blocking of the sample while waiting for the following hold (blocking); association of an entire value to the sample (quantification), coding the value into binary (digitalization).

The first operation holds the sample of the signal s (t). Operation is repeated with equidistant temporal intervals controlled by a sampling clock of period Te. Each sample is located by its sequence number N (positive entire) at the moment nTe. It's noted S (nTe) or S (N). The building block carrying out this operation is called sampler:

A. Sampling

When wishing to digitalize an analogical signal (continuous in the time), i.e. to code it utilizing a finished succession of numbers we, generally, start by sampling it, except in the case of very slow signals compared to the sampling rate. This operation consists in holding to the instantaneous value of the signal with intervals separated by a time constant **Te,** called period of sampling. At the output of the sampler, the values of the original signal are known only all **Te** seconds.

Then, to be able to reconstitute the original signal starting from the samples taken at discrete moments, it is necessary to choose a sufficient number of samples. Signal will be studied according to the frequency, respecting the Shannon theorem. In order to guarantee the faithful restitution of the original signal, the theorem of sampling (Shannon theorem) stipulates that the sampling frequency must be greater or equal to the double of the maximum frequency of the signal. Otherwise, we observe the phenomenon of folding up; the low frequencies interfere with the high frequencies

B. Principle of the Temporal Sampler

The goal of this operation is to digitize the original analogical signal. To achieve this goal, we must take at certain points samples of original signal, regularly distributed temporally. This operation is thus accompanied by a loss of information. To reduce at the maximum the loss of information, we must increase the number of samples. If (Te)

is the period of sampling, (K) the number of the samples and (te) the time of sampling then $t_e = k.T_e$
Sampling consists in representing a continuous analogical signal x (t)) by the entire values x (k*Te).

The analogical switch is ordered by a clock when utilizing a low frequencies generator connected at the output of impulses. The clock delivers an impulse of 5 volts at the regular interval.

The clock allows to close the analogical switch and to carry out the sample.

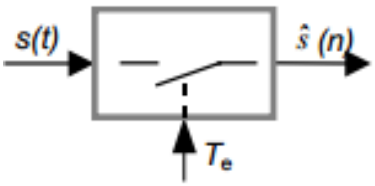
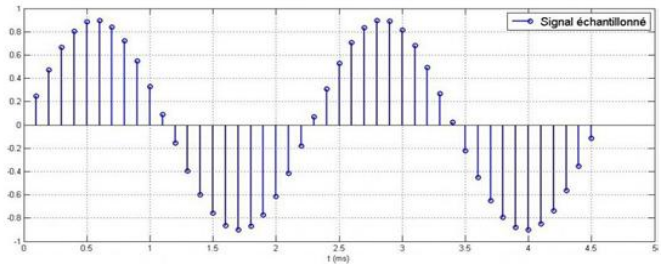


Figure -8: Sampler-temporal



Sampled signal

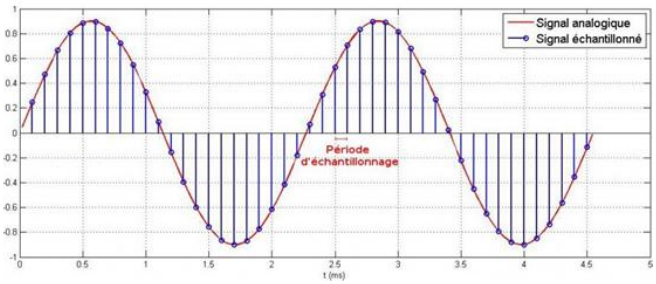


Figure- 9: Analogical and sampled signal

Before taking a new sample, it is necessary to maintain the present one (s (n)) during a certain instant (corresponding to the conversion time). To enable that, we use a blocker as "analogical memory". The obtained signal is noted s*(n) (see figure below).

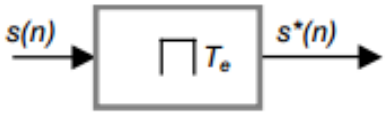


Figure- 10: Blocker

The role of a sampler-blocker is to maintain constant the amplitude of the sample taken every te seconds during a time necessary for the conversion.

C. Realization of the sampler-blocker

The two operations (sampling and blocking) are associated in the same technological block; it is the sampler-blocker (or sample and hold in Anglo-American). The principle structure is given on the figure below:

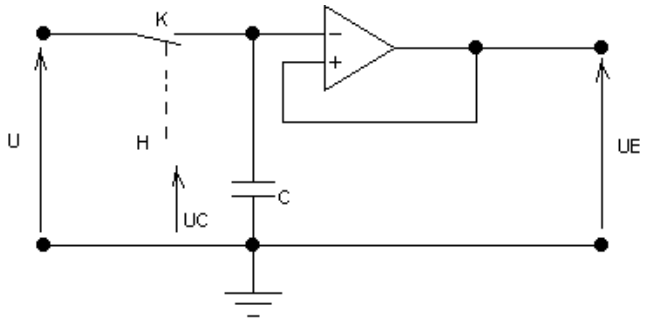


Figure- 11: Circuit of a sampler-blocker

According to the figure above, K is a switch ordered by the tension Uc. The period of the signal Uc is the period of sampling.
If Uc is in a high level, K is closed and the condenser takes care up to the value of U.
If Uc is a low level, K is opened and the condenser maintains a tension constant.

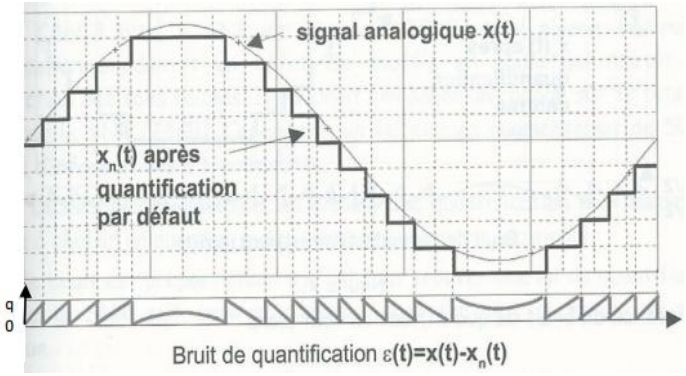


Figure - 12: Quantified signal

q represents the step of quantification. It is necessary to represent a word N having a great number of bits (small step of quantification). In fact, more q is small better is the precision. The amplitude of the signal is, at every moment, measured with an uncertainty ± q/2
The value of q is incompressible, it exists an equivalent theorem to that of the quantification which allows calculation of the exact value of the tension at the input. We call noise of quantification, the error made on a signal from an analogical-to-digital converter.

D. Quantification

The digital-to-analogical converter carries out the digitalization of an analogical signal after sampling and delivers digital sequences coded with a step of quantification q, which depends of the number of bits N of the converter. In the absence of knowledge a priori of the law of probability of the signal or when the quantification must be applied to various types of signals, we utilize a law of uniform quantification.

For a law of the uniform quantification where the coded values are obtained by rounded, we utilize a full scale of the analog-to-digital converter.

E. Coding

The sampled and quantified signal in amplitude is generally represented in binary format. If each number counts N bits, the maximum number of quantified amplitudes is 2^N. Then the range of the amplitudes which it is possible to code is subjected to a double limitation: towards the low values by $2^N * Q$.

Any amplitude which exceeds this value cannot be represented and there is chopping of the signal. It follows degradation, for example the harmonic distortion if the signal is sine.

Sampling is characterized by its period Te

$$F_e = \frac{1}{T_e}$$

Te is a minimum time necessary to the converter to stabilize digital data at the output when we apply a stable analogical tension at the input of a ADC. This characteristic fixes the maximum frequency of work.

According to the Shannon Theorem, the sampling rate (Fe) must be at least double greater of frequency (F) contained in the signal to sample: $Fe \geqq 2*Fsignal$.

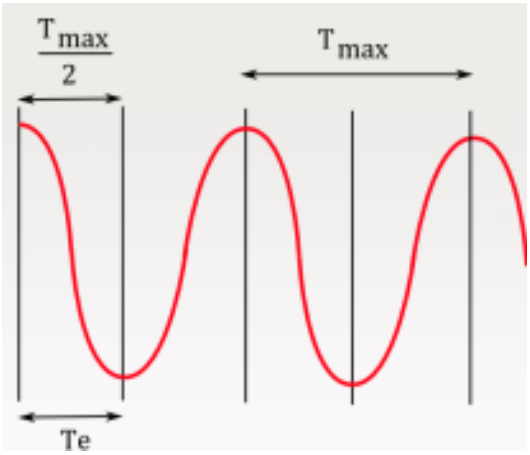


Figure – 13: Sampling rate

V ANALOGICAL-TO-DIGITAL CONVERTERS

There is more and more request concerning control by data processing of the physical systems. The problems related to the design of these systems lie in the realization of the interfaces to enable to recover a signal in order to read, to treat, and then to retransmit it in a second signal with different nature. The majority of the signals, to be treated are analogical; i.e. they vary continuously according to the time.

Thus, it will be necessary to use an analog-to-digital converter to connect physical phenomenon to the data-processing system. In addition, an digital-to-analog converter, will be necessary to reconvert data to the physical phenomena.

The DAC which convert the logical signals into analogical tension is indeed divided into two distinct fields:
The analogical field, where the variables can take an unlimited value; the signals vary continuously. All the signals from the sensors are analogical.
The digital field, where the variables take a limited states. At the base, signals have an analogical nature.

They should be amplified and extracted out noise. Sometimes, we need an analogical signal at the output of the data processing sequence: It will then be necessary to reconvert digital data to analogical signal.

The analog-to-digital converter converts a physical parameter (tension, current) into a binary number which is proportional to the physical parameter.

It is a system which, periodically takes and quantifies samples from an analogical signal. The digital value is then assigned to the taken and quantified samples. This quantification allows a digital secondary treatment of the collected data. This is why, according to the concerned application, the characteristics of the analog-to-digital converter vary simultaneously in terms of precision, resolution (linearity), speed of sampling and the energy consumption.
An analogical-to-digital converter is used mainly as interface between a sensor and a microcontroller. Signals can vary very slowly (temperature) or very quickly (audio signal).

During the conversion process, the analogical-to-digital converter compares the present signal at its input to the subdivisions and decides with which subdivision the value of the sample belongs and sends at the output the suitable binary code. The number of bits of the binary word at the output is called resolution of the analogical-to-digital converter. Comparisons between analogical signal to references are carried out using one or more comparators, depending on the type of converters. A comparator is a component which compares two values, analogical or numerical, present in its input and deducts the bigger one, then decides to send a logic 0 or 1 at its output.

There are various techniques of DAC: Converters with integration (Simple ADC crawls, Double ADC crawls, ADC delta-sigma); Converters with counting (ADC with digital slope, ADC with continuation, DAC with conversion Tension / Frequency).

Other techniques of conversion (ADC Flash, ADC with approximation successive, Converter with successive approximations SAR, Converter FLASH, Converter on multiple floors, Cyclic Converter Pipeline, Converter Sigma-Delta).

PARALLEL CONVERTER OR FLASH

A Flash converter of N bits of resolution consists of an entire of $2^N - 1$ comparators and signals of reference.

Each comparator compares the signal sampled with one of $2^N - 1$ reference signals. Thus, each comparator generates an output signal which indicates if the signal is higher or lower than the reference signal. These multiple comparisons carried out in parallel, permit to determine the beach in which is located the signal to be digitized.

The principal disadvantage of this architecture is the significant number of comparators and references necessary when the desired resolution is large. It will require an increase of used surface, of input consumption and of capacitance. For example, for 10 bits, we need 1023 comparators and reference of tension. Moreover, for such resolutions, the offsets errors of comparators and of references must be lower than the desired resolution.

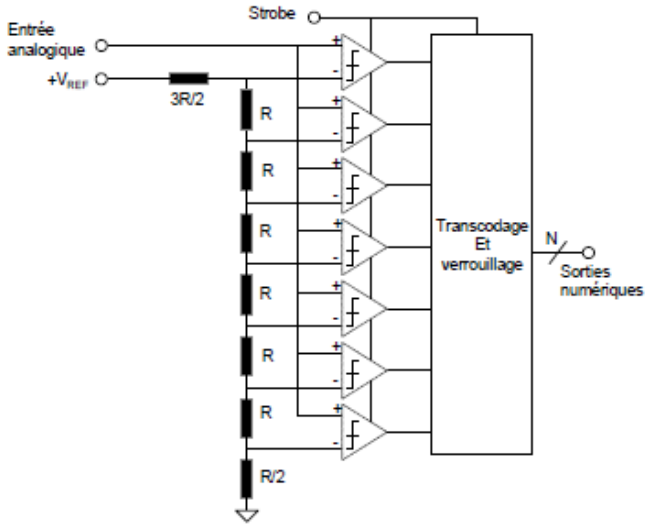


Figure – 14: Parallel analogical-to-digital converter or flash

In the principle, this type of ADC could be relatively precise. However, in practice consumption energy is important. If the input varies quickly, the output becomes unstable. According to the linearity, there is dispersion on resistances and the comparators. In addition, there is a great dependence with the quality of V_{REF}.

We need 2^N - 1 comparators for N bits, that is to say 8 comparators for 3 bits and 255 for 8 bits. The process thus becomes quickly restrictive.

The principal source of error comes from the offset of the comparators which introduce non-differential linearity. The speed is conditioned by the speed of the comparators and that of the logical decoder. The rate of conversion can reach hundreds of MHz for the numerical oscilloscopes.

These ADC are limited to 6 or 8 bits, which is insufficient for instrumentation. This handicap is negligible numerically. Utilizing oscilloscope, certain manufacturers use 6 bits converters, which is sufficient to describe the vertical axis of the screen with a resolution higher than 2%.

For applications requiring no very high speeds, we use semi-parallel converters, which use much less comparators and preserve an enough speed of conversion with a resolution able to reach 12 bits.

VI. SIMULATION

A. Presentation of Software

Figure – 15: Proteus-ISIS simulator

An electronic simulator is a software modeling the operation of electronic circuits in order to be able to envisage and analyze their behavior. There are various levels of simulation, according to the degree of smoothness and the scale of simulation. To simulate our electronic circuit, we use software ISIS of Proteus.

It's mainly used to draw electric diagrams in order to detect certain design errors. In documentations, it controls the majority of the graphic aspect of the circuits.

The software ARES is a tool of edition and routing which completely perfects ISIS. An electric diagram carried out on ISIS can then be imported easily on ARES to carry out the printed circuit although it will be more efficient when it is carried out manually. The software places the components automatically and carries out also the routing automatically.

B. Environment of Work of Isis

We did our simulation under the environment of work of ISIS Professional version 7. Figure below shows its interface.

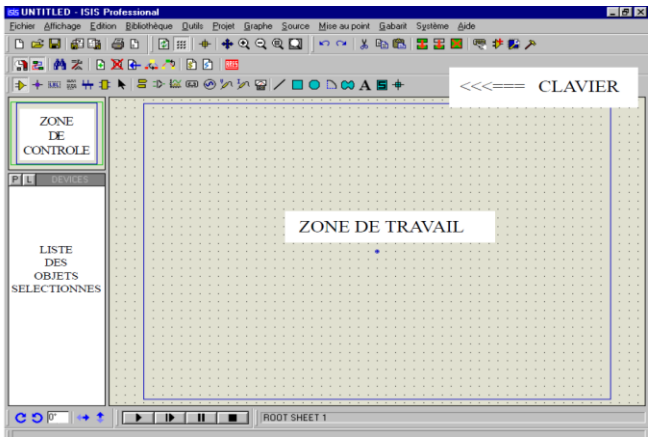


FIGURE – 16: The environment of work of ISIS Professional version 7.

C. ADC 8 BITS

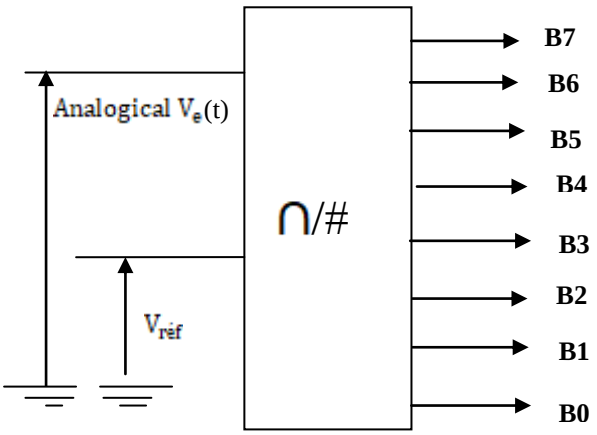


Figure – 17: Symbol of the analog-to-digital converter

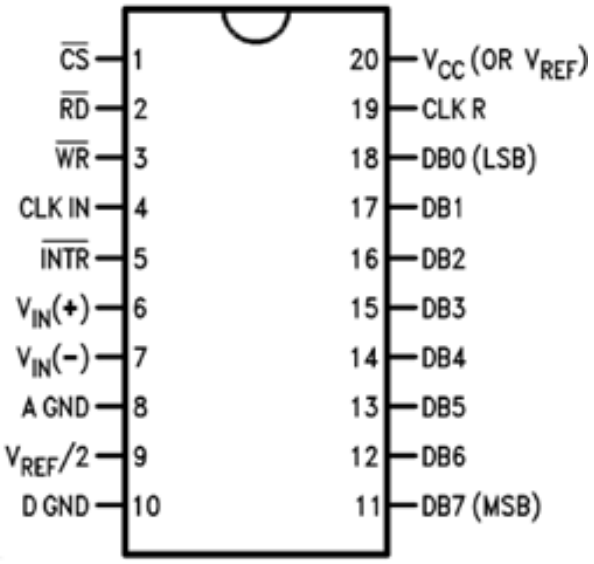


Figure – 18: Integrated circuit of ADC0804

Circuit ADC0804 is an ADC by successive approximations, which can be easily connected to a microprocessor 8088. It converts analogical tensions from 0 to 5 Volt into a numerical value coded on 8 bits.

D. Principal Characteristics of Circuit ADC0804

8 bits of resolution;
Parallel ports;
The single supply voltage + 5 V;
Differential Inputs (0 To + 5 V);
frequency of clock up to 1 MHz;
Sampling rate: 14 KHz (with a clock of 1 MHz);
With Ve = 0 V, the output gives (0000 0000);
With Ve = 5 V (full scale), the output gives (1111 1111);
the logical level to apply to C S = Chip select to validate the controller C S;
Compatible with all the microprocessors;
Outputs 3 states;
Logical levels: compatible TTL and MOS;
Can use internal or external clock.
INTR **(INTeRrupt):** the signal passes to 0 as soon as a conversion is finished and the digital data is ready (available on the bits of output).
WR (Write): This input starts conversion when it is put in its active state.
Pins from 11 to 18: Digital displays.
If CS and RD are equal to 1, then the outputs are on the state high impedance (open State).
WR acts like line of control when CS = 0 and conversions are started.
INTR allows announcing the end of conversion.
Vin+ and Vin- are the differential analogical inputs.
CLK IN is the input of the clock signal.
CS (Select Chip): Mean "selection of the circuit": its setting in an active state inactive the circuit i.e. puts its outputs in high impedance; that disconnect them from the assembly. The setting in high impedance of the outputs proves to be essential when the logical analyzer is in reading mode: The data bus is then used at output and does not have to be connected to the outputs of the ADC.

This command is very useful in the microprocessor assemblies in which the address and data buses are divided by a great number of integrated circuits.

This setting in high impedance can also be carried out starting from the reading command $\overline{RD}$ of ADC. The use of the input CS is not then more essential and we can activate the circuit permanently, i.e. put $\overline{CD}$ in his active state.

$\overline{RD}$ (ReaD): Is the reading command. In active state, the outputs pass from the high-impedance mode to the mode data-available. It is used to put the outputs in high impedance during the reading in the logical analyzer, to avoid connexion between 2 outputs (outputs of the logical analyzer and the ADC).

Because the converter used functions by successive approximations, and consequently required a clock to increment its internal meter. This clock can be external or internal (see paragraph "clocking options"). In this last case, a resistance and a condenser must be used; they form with a reverser door with hysteresis (intern with the circuit) an assembly astable which generates this clock signal.

Table: Electrodes of the integrated circuit ADC0804

1	$\overline{CD}$	Chip Select, selection of the circuit, (active on the low level)
2	RD	Read (active on the low level)
3	WR	Write (active on the low level)
4	CLK IN	Input of the Clock
5	$\overline{CD}$	The switch, which ends conversion
6	$V_{IN}+$	Input of the analogical signal
7	$V_{IN}-$	Output of the analogical signal
8	AGND	The ground connection of analogical signal
9	$V_{REF}/2$	Half of the reference voltage standard
10	B GND	Mass of the circuit
11	VCC or V_{REF}	The supply voltage of the circuit
12	CLK OUT	Output of the Clock
13	DB0 (LSB)	Bit 0 (Least Significant Bit)
14	DB1	Bit 1
15	DB2	Bit 2
16	DB3	Bit 3
17	DB4	Bit 4
18	DB5	Bit 5
19	DB6	Bit 6
20	DB7 (MSB)	Bit 7 (Most Significant Bit)

E. Reference voltage standard V_{REF}

It permits to define the value of the quantum ADC 8 bits:
$0V < V_{REF} < 5$ V

The variation of the output (ΔV_0), is the variation of the output when the input varies from 1, less significant bit (LSB):

$$V_{REF} = 2^N . \frac{V_E}{N_X} \quad (16)$$

For

$$V_E = V_{max} \quad (17)$$

$$N_X = N_{max} = 2^N - 1$$

thus

$$V_{REF} = V_{Emax} = 5V \quad (18)$$

For

$$N_X = 1 \quad (19)$$

$$q = V_E = \frac{V_{REF}}{2^N} = \frac{5}{256} = 19.53125 \text{ mV}$$

Maximum output V_{fs} is not equal to the reference:

$$V_{fs} = V_{réf}\left(1 + \frac{1}{2^N}\right) \quad (20)$$

Clock of sampling, will increment the addresses of the logical analyzer. Since a data can be memorized as soon as it is converted, we use for this clock output $\overline{INTR}$ of the ADC.

f_{CLK} is a function of the frequency of desired conversion. The manufacturer gives the typical f_{CLK} frequency.

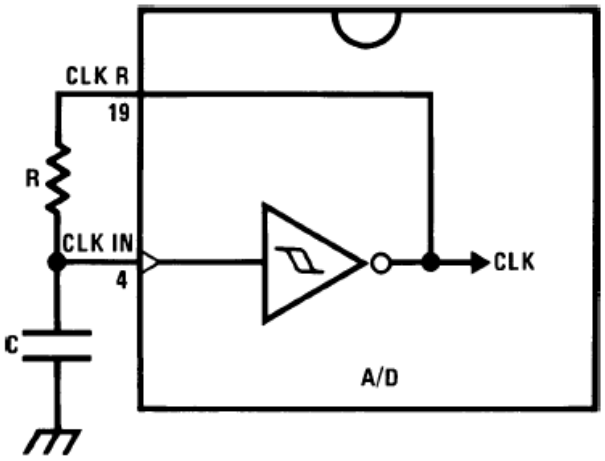


Figure – 19: Realization of clock in the ADC

To produce the clock corresponding to our assembly, it is necessary to seek the values of R and C allowing the correct operation of our realization. These values are given according to the formula given in the datasheet.

$$f_{CLK} \approx \frac{1}{1.1RC} \quad \text{: Where RC is the time constant} \quad (21)$$

$$I_R >> I, donc \ R < R_{MAX}$$

C gives the maximum of dynamics at the output of the integrator.

The manufacturer gives the values of CTYP and RTYP according to the beach of V_{REF}.

1 MΩ and 100µF are the reasonable values of R and C. The maximum value that can take the frequency of the clock as well as the number of periods of clock, which requires 1 conversion, can then be calculated from the above values. Obtained number indicates the maximum sampling rate of the system. It must be checked, in particular, that the sampling rate imposed by the schedule of conditions can be reached with this converter.

Since the ADC comprises an internal generator of clock, it should be interesting to use it in order to give rhythm to the remainder of the assembly; to avoid thus a clock block.

Since we seek to have a given frequency of conversion (Féch), it is necessary to arrange the situation in order to have as duration of conversion (1 /Féch). In other words, signal $\overline{INTR}$ announces the end of a conversion every (1/Féch).

An analogical-to-digital conversion (correspondent with 1 digital data) requires a cycle read-write. According to the chronogram of ADC Document, a new conversion starts when the input $\overline{WR}$ passes in its active state (i.e. 0). When the conversion of a data is finished, the output $\overline{INTR}$ passes to 0.

To function in autonomous mode, it is necessary to buckle the output $\overline{INTR}$ on the input $\overline{WR}$. As soon as the conversion of a data is finished, the conversion of a new data starts automatically. In fact, because the propagation time of signals in the circuit is not null, an analogical-to-digital converter can function in autonomous mode. Indeed, according to the chronogram below, while $\overline{WR}$ passes to 0, the output $\overline{INTR}$ is shifted to 1, and that one is rebuked on the first. Thus, because there is a time of approximately 300ns between the passage of WR to 0 and the passage of $\overline{INTR}$ to 1 this mode is possible: otherwise $\overline{INTR}$ will not have enough time to go down to 0 and would be thus not exploitable.

However, to engage this cycle, we apply a short impulse to 0 at the input WR; that can be carried out by bringing the mass by a switch (or a simple wire) at this input.

This method is not rigorous, because it connects the output $\overline{INTR}$ to the mass and thus short-circuits it. However the test is indicated and guaranteed by the manufacturer. The rigor would like that we combine the switch with the output $\overline{INTR}$ by a gate AND.

Conversion time (Tc) is equal to: $Tc \approx 2*2^N*T_E$

It depends on the technology, i.e. of its internal structure. It must be lower than the sampling period ($Tc < T_E$) of the signal e (t).

$F_E = 1/T_E$, is limited by the ADC. The order of magnitude of Tc is: Tc = 100 ns for an ADC 8 bits.

For ADC0804 - 8 bits, Fe = 1/100 µs = 10 KHz (10 000 samples per second)

F. Integrated Circuit of ADC0804 Containing an ADC with Successive Approximations

This circuit is supplied by +5 V, has a resolution of 8 bits with a conversion time of 100 µs. It contains a generator of clock signal integrated. The outputs of data are in three states and can be put in interface with the buses of a microprocessor-based system.

The operation of circuit ADC0804 is equivalent to that of an ADC network with 256 resistances. Logic by successive approximations crosses the network to equalize the input differential tension (VIN^+ - VIN^-) by determining an output in the resistive network.

A binary code of eight bits is transferred to the output bolts and the output of interruption $\overline{INTR}$ passes on the low level. The component can also function in free mode by

connecting the output $\overline{INTR}$ to the writing input $\overline{WR}$ and by maintaining the starting pin of conversion CS on the low level. Under any conditions, to $\overline{CD}$ start Ci, we place on the low level the input $\overline{WR}$ when the component is supplied. A low level on CS interrupts the conversion cycle.

When the input $\overline{WR}$ passes at the low level, the register with successive approximations and the shift register of eight bits are re-initialized. The ADC remains at the state RESET as long as a low level is maintained at the inputs $\overline{CS}$ and $\overline{WR}$.

The conversion starts between the first and the eighth period of clock signal after transition from low level to high level of $\overline{CS}$ or of $\overline{WR}$.

When we apply a low level at the inputs $\overline{CS}$ and $\overline{RD}$, the output bolt in three states is validated and the output code is placed on the lines from D0 to D7.

When one of the inputs $\overline{CS}$ or $\overline{RD}$ passes at the high level, outputs from D0 to D7 are then blocked.

G. Visualization of the Signals on ISIS

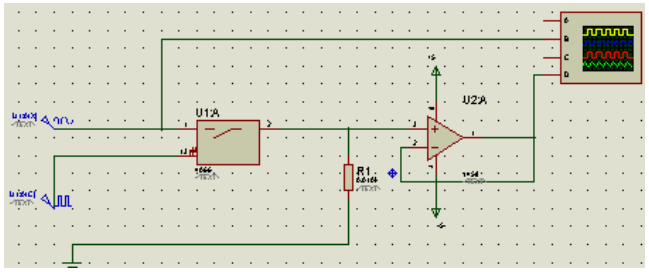


Figure – 20: Sampler Circuit

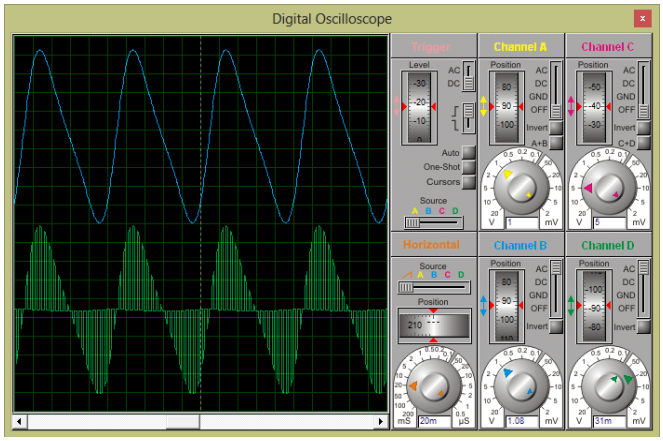


Figure – 21: Analogical and sampled signal on oscilloscope

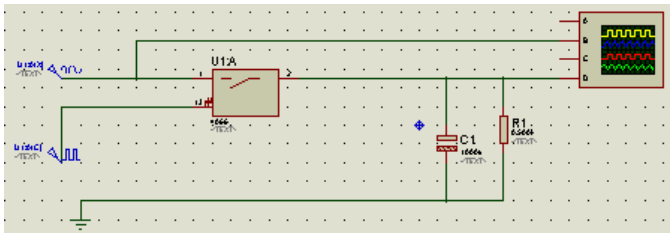


Figure – 22: Sampler-blocker

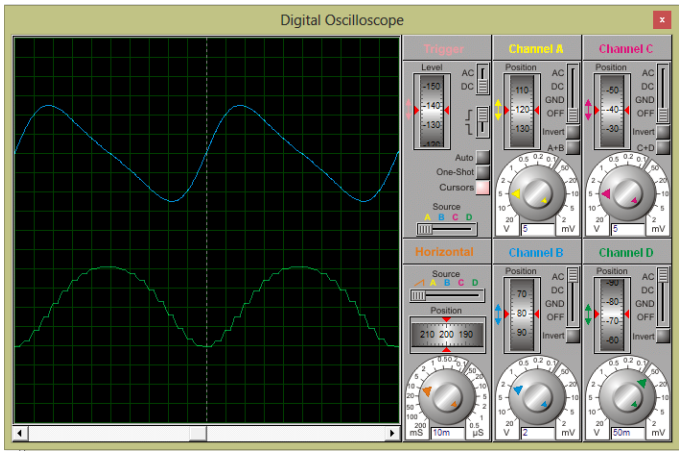


Figure –23: : Analogical and quantified signal on oscilloscope

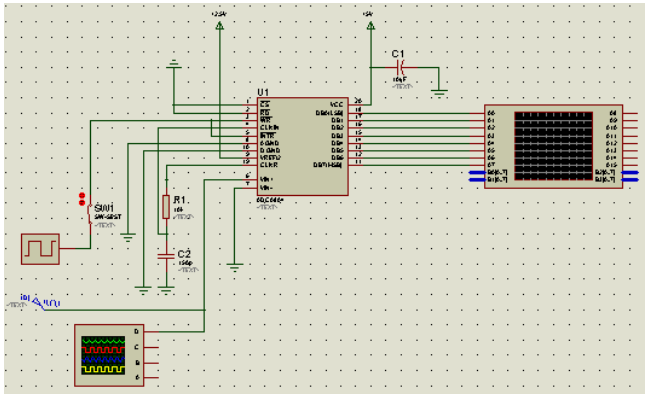


Figure – 24: Diagram of the ADC 8 bits with ADC0804 circuit

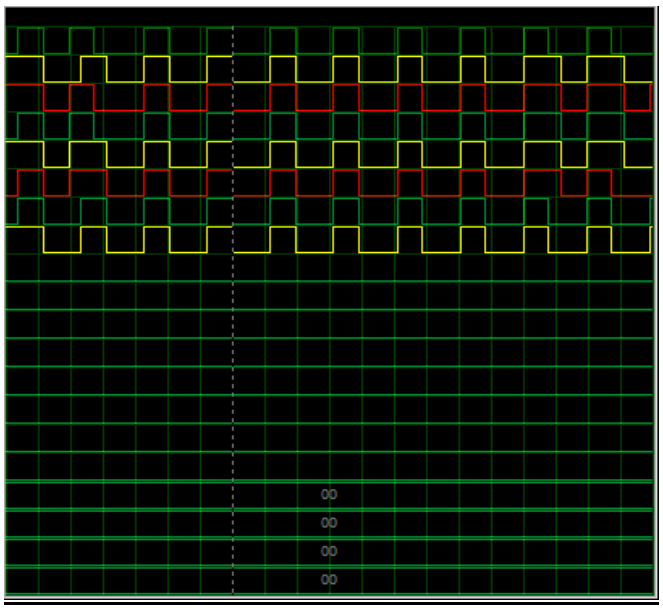


Figure – 25: Digitalization of the signal of 8 bits on the logical analyzer

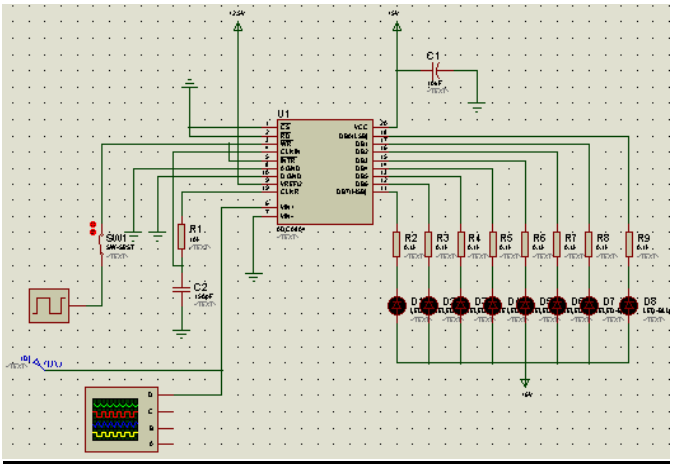


Figure – 26: Realization of an ADC ADC0804 8 bits with the LED on ISIS

VII. ADVANTAGES AND APPLICATIONS

A. Analogical-to- Digital Converters

In the measurement equipments and test, the ADC are utilized to digitize the signals at the output of the test module, to store signals in the hard disk being used for the data acquisition or for display on a screen. Examples of such equipment are logical analyzers, oscilloscopes and analyzers of spectrum. The numerical oscilloscopes and the logical analyzers, most powerful, typically utilize an ADC of 8 bits implemented with bipolar technology or Gallium Arsenic (GaAs).These analog-to-digital converters generally operate with some Giga Samples Per Second (GSPS). Until our days, these technologies offer unequalled performances in terms of speed in comparison with CMOS technology.

The conceived ADC consume enormously power, which limits their applications. Whereas the aspect of consumption is not very critical in the field of the testing equipments, it is of fundamental importance in projects of wireless systems.

The systems of storages to magnetic medium for hard disks with great densities require an ADC having an accuracy of 6 bits and a conversion rate higher than 1 GSPS in order to allow an effective reading of the input channel. It is expected that this conversion rate will increase in parallel with the growth of the density of storage with the time. Accordingly, the ADC must be fast and must have low power consumption, particularly with the development of the hard disks dedicated to the portable computers.

The ADC allowed considerable progress in the world of the numerical communication. There are several types of architecture of radio operator receivers like the heterodyne receiver, the homodyne receiver, the receiver- IF and others. Most known is certainly the heterodyne receiver. Its architecture functions in 3 stages of frequencies: the level of the radio - frequencies RF, the level of intermediate frequencies IF and the baseband (Low Frequencies). However, architecture is of a great complexity and consequently, requires a great consumption of power.

The concept of "radio configurable operator" is defined by the software SDR (SDR- Software Define Radio). The goal is the adaptation to the various standards of wireless communication. These SDR systems radio operator are used for a direct conversion. They must be flexible, reprogrammable. To achieve these goals, the receiver by radio operator must directly digitalize signal RF on the output side of the reception antenna, to allow software to numerically treat the signal and to reprogram the receiver on another frequency.

In opposite to the heterodyne receiver, the SDR system must be very fast in order to take at real time signal RF so that the consumption of power is minimum and to satisfy the criterion of portability. In fact, the SDR concept calls upon an extremely powerful ADC.

The applications in which analogical data must be digitized and transferred in a memory of computer are numerous. The process of seizure by the computer of the digitized analogical data is called the data acquisition.

When we utilize a computer to memorize an analogical data (it is the case of a numerical oscilloscope), that one stores the data then transfers them to a DAC so that it reproduces the analogical data. It exists ADC in the numerical multimeters, the systems of acquisition, the development of the matrix of a compact disk....

We utilize ADC0804.8 bits as interface sensor microprocessor; digital thermometer; thermostat with digital control; monitoring and system of control containing microprocessor.

It is possible to program the computers so that they produce the analogical signals necessary to test the analogical circuits. The analogical response of the circuit will be converted into numerical value by an analogical-to-digital converter and will be reintroduced in the computer.

B. Digital-to-analogical

We utilize the digital-to-analogical converters in order to transform the digital display of a circuit into an analogical tension involving an analogical device. Some of the most current applications are:

The digital display of a computer is converted into an analogical signal in order to regulate the speed of an engine, the temperature of a furnace or to order an unspecified physical variable. The command of the machines is a sector where the digital techniques are required.

We can also utilize a digital - to - analogical converter to numerically regulate the amplitude of an analogical signal. A typical application of a DAC is the numerical “adjustment of volume”, in which the output of a digital circuit or a computer is used to regulate the amplitude of an audio signal after conversion.

In addition, we find the DAC in the CD readers, in the systems of acquisition and the modems.

VIII. CONCLUSION

The analog-to-digital converters occupy a crucial place in the electronic circuits. The architectures are different by their speed of operation, their precision, their flexibility and their consumption of energy. The choice of the architecture depends of the nature of the application. Although f the field of research binds to the ADC is very active, architectures of the standard converters satisfy with difficulty the characteristics of the applications of low power, absorbing only some nW. It is the case of applications dedicate in particular to the sensors of signals, interfaces sensor - microprocessor, digital thermometer and the optical imagery. The converters with successive approximations seem to be more adapted for these types of application, because of the reduced number of active analogical circuits that they require.

Nevertheless, they are sensitive to the shift of the comparator and the linearity of the ADC which affects their performances. Moreover, except for the sampling frequencies less than 100kE/s, the power which they dissipate in the case of 8 bits surplus the range of n²W. We utilize ADC0804.8 bits as interface sensor microprocessor; digital thermometer; thermostat with digital control; monitoring and system of control containing microprocessor in the CD readers in the systems of acquisition and the modems.

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Publications: "ASICON IEEE 2005, 734-738", "HIT journal 2006 13(3) 251-254", "WSEAS Transanction on Circuits and System 2006 5(3) 640-646".