International Journal of New Technology and Research (IJNTR)
ISSN:2454-4116, Volume-3, Issue-10, October 2017 Pages 92-96

Improving the performance of Five Level Inverter With Grid Interfaced under Various Events of Power Quality

Dr.B.Gopinath, Mr.M.Kalyanasundaram, V.Karthika, M.Pradeepa

***Abstract*— This paper presents adaptive synchronization based dq-current control technique for five-level NPC grid interfaced inverter DG system. Due to synchronization the performance of grid interfaced DG systems affected by power quality (PQ) events such as, balanced and unbalanced voltage sag/swell, frequency shift, phase jump and harmonic distortions .An amplitude adaptive notch filter (AANF) is used for detection of utility voltage phase angle and estimate frequency, amplitude .In this proposed paper the five level inverter is used to reduce harmonic distortion. This technique also operates interfacing inverter close to UPF mode. The efficacy of the proposed control technique in integrating the DG system under PQ events to the utility grid is investigated through MATLAB simulation results. The laboratory experimentation is ongoing and can be presented latter**.

***Index Terms*— Grid synchronization, grid interfaced inverter, DG systems, power quality improvement.**

I. INTRODUCTION

Distributed generation system is the term used for interconnection of renewable energy sources to the distribution grid[1]. This novel concept of renewable energy integration is gaining major share in the current electricity market due to enormously increasing clean energy demand. However, these grids integrated DG systems and continuously increasing non-linear loads are the basic sources of power quality related issues in the electricity distribution network [2]. Therefore, interconnection of such DG systems demand
advanced current control strategies to enhanced power quality. However, penetration of high quality power generated by these DG systems mainly depends on extraction of synchronized pure reference current signals for grid interfaced inverter exclusively under various power quality disturbances. In order to achieve enhanced control performance, fast and accurate detection of fundamental unit voltage vector of the utility grid voltage at PCC is very necessary. In addition, the DG system control circuit should also maintain robustness and stability under various PQ disturbances in order to meet standard grid codes [4].

To meet standard grid code requirements design of adaptive control technique under sudden PQ-events is the most important part of grid interconnection of DG systems. Along with injection of generated active power, reactive power and harmonics current compensation for power quality (PQ) improvement under various PQ disturbance conditions is also one of the important issues in control of DG systems. A
multipurpose current control technique for conventional voltage source inverter (VSI) with power quality improvement features is explained in [5].

An enhanced current control approach with non-linear load harmonic mitigation capabilities under frequency shift is presented. In [6], author has presented an adaptive synchronization based current control technique for interconnection of DG systems with improved power quality feature. In this paper, performance improvement of grid interfaced five-level inverter DG system under various PQ disturbances is presented.

Adaptive synchronization based *dq*-current control technique for five-level NPC grid interfaced inverter DG systems is proposed. Three phase extension of single phase AANF is developed for detection of utility voltage phase angle due to its adjustable accuracy and amplitude adaptability [7]–[9]. The control circuit is designed such that DG will only inject active power and maintains power factor close to UPF as per the IEEE 1547 standards. Performance of the proposed control technique in injecting the active power into the utility grid under PQ disturbances is investigated through MATLAB simulation results.

II. FIVE-LEVEL DIODE CLAMPED INVERTER DG SYSTEM UNDER STUDY

The 5- level diode clamped multilevel inverter uses switches, diodes; a single capacitor is used, so half of the input DC. The five-level converter in which the dc bus consists of four capacitors C_1, C_2, C_3 and C_4. For dc bus

Dr.P.Gopinath.,M.E.,Ph,.D, Vivekananda college of engineering for women, Tiruchengode , India
Mr.M.Kalyanasundaram, M.E.,(Ph.D)., Vivekananda College of engineering for women, Tiruchengode, India
V.Karthika.,PG student , Vivekananda College of engineering for women, Tiruchengode, India,
M.Pradeepa.,PG student , Vivekananda College of engineering for women, Tiruchengode, India,

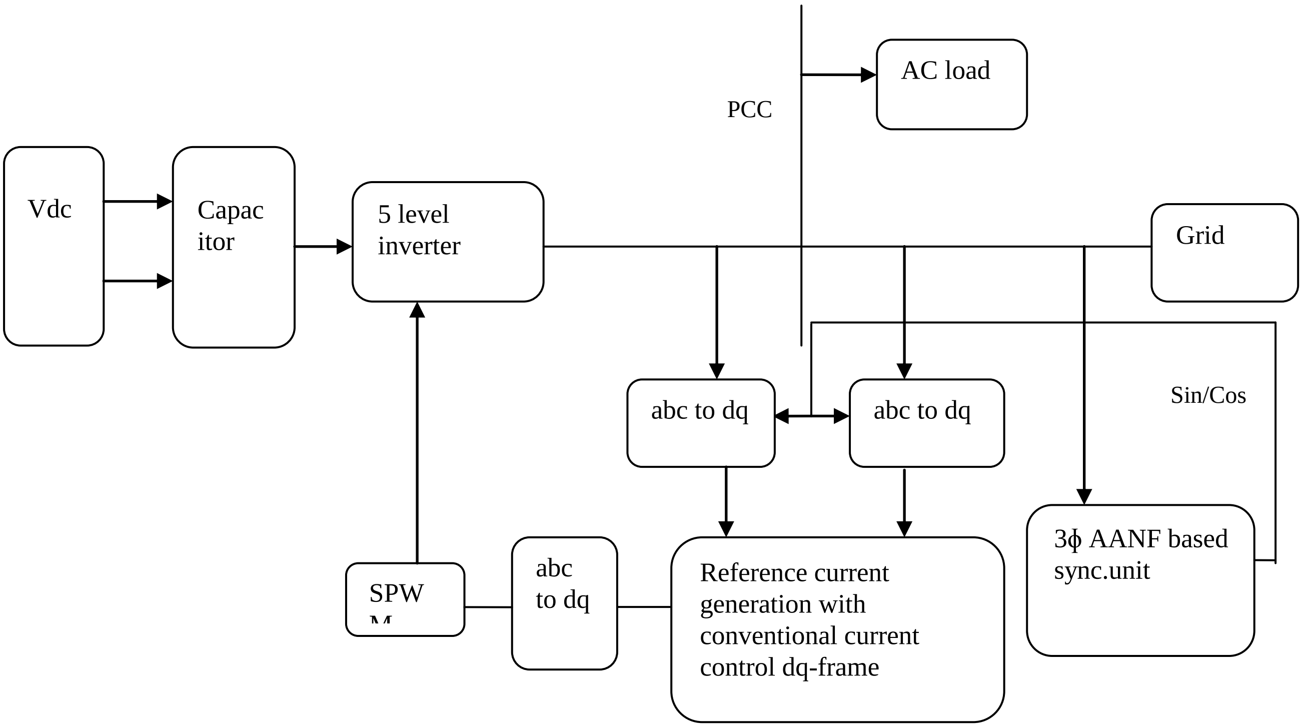


Fig. 1.Block diagram of five level diode clamped inverter interfaced DG system.

voltage V_{dc}, the voltage across each capacitor is $V_{dc}/_4$ through inverters. There are five switch combinations to synthesize five level voltage across a and n in [11].

1) For voltage level $V_{an} = V_{dc}/_2$, turn on all upper switches$S_1 - S_4$.

2) For voltage level $V_{an} = V_{dc}/_4$, turn on three upper switches $S_2 - S_4$ and one lower switch $S_1^{'}$.

3) For voltage level $V_{an} = 0$, turn on two upper switches $S_3 - S_4$ and two lower switches $S_1^{'} - S_2^{'}$.

4) For voltage level $V_{an} = -V_{dc}/_4$, turn on one upper switch S_4 and three lower switches $S_1^{'} - S_3^{'}$.

5) For voltage level $V_{an} = -V_{dc}/_2$, turn on all lower switches $S_1^{'} - S_4^{'}$.

III. THREE PHASE AANF

Adaptive and robust synchronization is very important in order to improve the performance of grid connected DG systems under various PQ-events. Here, three phase extension of AANF is developed for detection of utility voltage phase angle and generation of fundamental unit voltage reference signals. Single phase AANF is used because of its adaptability under adverse grid conditions [7], [8]. An input grid voltage signal is represented as,

$$V(t) = \sum_{i=1}^{n} A_i sin\emptyset_i \; where, \emptyset_i = \omega_i t + \varphi_i \qquad (1)$$

Here, the frequencies ω_i , and the phases ϕ_i, where, i =1,2,3,.....,n, are unknown quanties. To estimate all these quantities an AANF structure proposed in [7] is represented as,

$$\ddot{x} + \theta^2 x = \sqrt{2\theta_e(t)}$$

$$\gamma = \frac{\epsilon}{(1+A^2)(1+\mu\theta^2)} \qquad (2)$$

Where, θ represents frequency. For a fundamental frequencyω_1, the periodic orbit of AANF

$$(0) = \begin{pmatrix} x \\ \dot{x} \\ \theta \end{pmatrix} = \begin{pmatrix} \frac{-A_1}{\omega_1}\cos\,(\omega_1 t + \varphi_1 \\ A_1 \sin\,(\omega_1 t + \varphi_1) \\ \omega_1 \end{pmatrix} \qquad (3)$$

Where, the element O gives the fundamental frequency ω_1 of the periodic input signal. This information is then useful for sequence component extraction in order to accurately detect utility voltage phase angle for control circuit design. For this, three identical AANF mathematical models described above are used to develop three phase AANF structure. A basic block diagram of the single phase AANF structure used to develop three phase AANF is as shown in Fig. 2. Three phase AANF structure is mathematically represented as,

$$\ddot{x_n} + \theta^2 x_n = \sqrt{2}\theta e_n(t)$$

$$\gamma_n = \frac{\epsilon}{(1+A_n^2)(1+\mu\theta^2)} \qquad (4)$$

Where, $n = a, b, c$ are three phases of sinusoidal input voltage signals. in (4) $x^{\cdot}_n = A_n \sin(\omega_0 t + \phi_n)$ and $-\theta x_n = A_n \cos(\omega_0 t + \phi_n)$ are the fundamental and its 90^o phase-shift component of the three phase input voltage respectively. These components are then represented by output column vectors $X_1(t)$ and $X_2(t)$ as,

$$X_1(t) = (-\theta x_a \quad -\theta x_b \quad \theta x_c)^t$$

$$X_2(t) = (\dot{x_a} \quad \dot{x_b} \quad \dot{x_c})^t \quad (5)$$

The three phase input voltage signals are decomposed into its symmetrical components by using (5) and a linear transformation proposed as,

$$V^0(t) = (I - 2T_2)X_2(t) \quad (6)$$

Where, I is an identity matrix. The transformation matrices T_1 and T_2 are given by,

$$T_1 = \frac{1}{2\sqrt{3}}\begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \quad (7)$$

$$T_2 = \frac{1}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ -0.5 & 1 & -0.5 \\ -0.5 & -0.5 & 1 \end{bmatrix} \quad (8)$$

IV. FIVE-LEVEL DIODE CLAMPED INVERTER CONTROL CIRCUIT

In the proposed control technique, three phase amplitude adaptive notch filter (AANF) is used as a synchronization unit for extraction of fundamental frequency and phase angle of

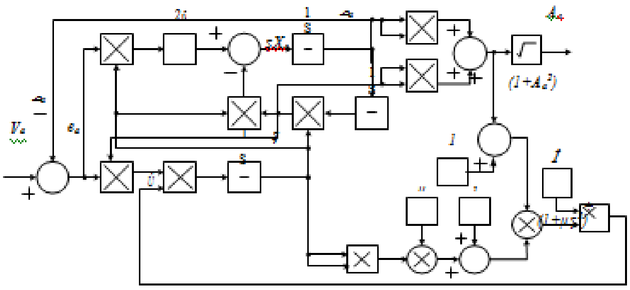


Fig. 2. Structural representation of AANF.

the utility voltage signal. In the conventional current control technique proposed, a SRF-PLL is replaced by ex-tended three phase AANF for performance improvement under various PQ-events. This control technique is designed to inject active power generated by DG systems into the utility grid and maintain UPF operation of interfacing inverter. Here, the extracted fundamental phase angle (θ) is used for estimation of sin(θ) and cos(θ) required for Park's transformation.

In order to operate DG system inverter in UPF mode, reactive power reference value (Q_{ref}) is assumed zero. Assuming the steady state condition, the active and reactive power supplied by the DG in *dq*-frame is given as,

$$P_{ref} = \frac{3}{2}[V_d \quad I_{d-ref}] \quad (9)$$

Here, for the simulation study, active power reference value (P_{ref}) is taken as 6kW. However, as the reactive power

reference value is set to zero (Q_{ref} = 0), $I_{q\ ref}$ is always zero. The actual output DG currents in *abc*-frame (I_{abc}) are transformed into rotating *dq*-frame (I_{dq}) using Park's transformation. These actual DG currents (I_{dq}) are then subtracted from the reference DG currents ($I_{dq\ ref}$) and the current error ($I_{dq\ ref}$) is regulated using PI-regulator.

The outputs of the PI-regulator are then added with the PCC voltages in *dq*-frame (V_{dq}) to get the modulating signals (M_{dq}) required to drive interfacing inverter. Level shifted carrier based SPWM technique is used to generate gate pulses for three level diode clamped inverter.

TABLE I

THE DG SYSTEM PARAMETERS

Sr.No.	Parameter	Value
1	Nominal grid voltage (V_G)	400V (L-L)
2	System frequency (f)	50Hz
3	Coupling inductance (L_c)	4.9mH
4	DC link voltage	750V
5	Switching frequency (f_{sw})	3150Hz

V.SIMULATION RESULTS AND DISCISSION

To verify the performance, the complete Five-level inverter DG system model described in the previous section is simulated using power system toolboxes in the MATLAB/Simulink environment. The DG system simulation parameters are tabulated in Table I.

A. Performance evaluation of three phase AANF

Here, a 3-Phase, 400V, 50Hz programmable voltage source in MATLAB is used to create the disturbances such as, balanced and unbalanced voltage sag and swell of 20%, phase jump of 30^o, frequency shift of ±3Hz and addition of 5th and 7th harmonics of 7% in the input grid voltage signal.

To observe the performance of three phase AANF, estimated fundamental phase angle (sin(θ)) is overlapped with actual scaled-down grid voltage signal under all aforesaid PQ-events. The AANF parameters are set to $\zeta = {}^{1}/_{\sqrt{2}}$,μ= 0.00001 andε= 100000. Initially performance of three phases AANF for phase angle estimation is verified and its effect on the DG system performance is evaluated later.

1) Harmonics distortions: In order to create harmonics distortions in the input grid voltage, a positive sequence 5th and 7th harmonics of 5% are added between t=0.35sec to t=0.45sec in all three phases as shown in Figs. 3(a).

2) Frequency shift: Later, a frequency shift of ±3 Hz is added between t=0.34sec to t=0.44sec in the grid voltage as shown in Figs. 3(b).

Simulation results shown in Figs. 3(a) shows fast and adaptive response of three phases AANF for phase angle detection under all aforesaid PQ-events. AANF accurately detects fundamental phase angle of the utility grid voltage without distortions which is then used for synchronization of grid interfaced three level inverter.

B. Performance improvement of grid interfaced Five level inverter

Improvements in the control performance of the proposed grid interfaced five level inverter DG system due to fast and accurate synchronization are demonstrated under various PQ-events. In this paper, the control circuit is designed such that DG will only inject a constant active power and maintains power factor close to UPF as per the IEEE 1547 standards under various PQ-events. For simulation study, DG system rating is taken as 6-kW. In order to operate the DG at UPF mode, active power reference value (P_{ref}) is set to 6-kW and reactive power reference value (Q_{ref}) is assumed zero.

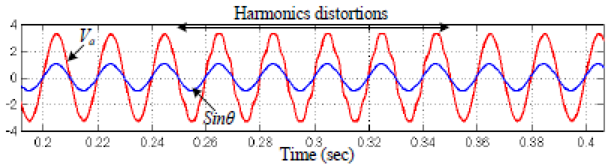
The actual values of DG active and reactive components of output currents are subtracted from the reference active and reactive components of currents and the error is passed through the PI-regulator to generate the modulating signals for five level inverter. This controls the injected active and reactive power generated by DG system. In this paper as the reactive power reference value (Q_{ref}) is assumed zero, DG will only inject constant active power (P_{ref}) into the utility grid. The performance of the proposed DG system in injecting a constant active power of 6-kW under various PQ-events is demonstrated as shown in Figs. 4.

The total harmonic distortion (THD) of the injected DG current is well within the IEEE 1547 standards under various PQ-events as tabulated in Table II.

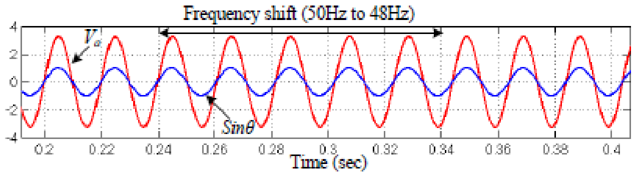
TABLE II

THD ANALYSIS OF DG CURRENT UNDER VARIOUS PQ-EVENT

PQ-Event	DG current THD(%)
Unbalanced voltage sag	2.14
Unbalanced voltage swell	2.14
Harmonics distortions	2.56
Phase jump	2.39
Frequency shift	2.35

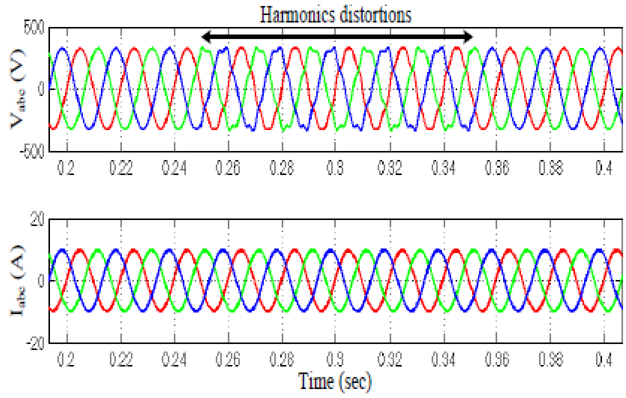


(a)Harmonicsdistortions.

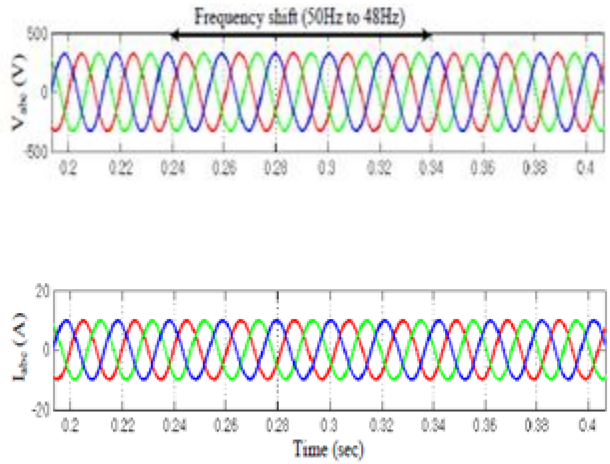


(b)Frequency change from 50 Hz to 48 Hz.

Fig. 3. Simulation results of three phase AANF for phase angle detection under various PQ-events (Y-axis scale: Grid voltage 100V=1V/div, sin(θ) 1V/div).



(a)Harmonics distortions.



(b)Frequency change from 50 Hz to 48 Hz.

Fig. 4. Simulation results showing performance improve ment in DG injected current under various PQ-events: PCC voltage (V_{abc}) and DG current (I_{abc}).

VI. CONCLUSION

This control circuit operates DG in UPF mode by injecting only active power into the utility grid. Robust behavior of three phases AANF enhances the control performance of the DG system. Three phase AANF based *dq*-current control technique for three-level NPC grid interfaced inverter DG systems is proposed. The proposed five level inverter is used to reduce more harmonics when compared to three level inverter . Performance of the proposed DG system in injecting the active power into the grid under PQ disturbances has been investigated through MATLAB simulation results.

REFERENCES

[1] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. PortilloGuisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso,"*Power-electronic systems for the grid integration of renewable energysources: A survey*," *IEEE Transactions on Industrial Electronics*, vol. 53,no. 4, pp. 1002–1016, June 2006.

[2] H. Abu-Rub, M. Malinowski, and K. Al-Haddad, *An Overview on Distributed Generation and Smart Grid Concepts and Technologies*.Wiley-IEEE Press, 2014, pp. 832–.

[3] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "*Multilevel inverters: a survey of topologies, controls, and applications*," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug 2002.

[4] F. Gonzalez-Espin, E. Figueres, and G. Garcera, "An adaptive synchronous-reference-frame phase-locked loop for power quality improvement in a polluted utility grid," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 6, pp. 2718–2731, June 2012.

[5] M. Singh, V. Khadkikar, A. Chandra, and R. Varma, "*Grid interconnection of renewable energy sources at the distribution level with power-quality improvement features*," *IEEE Transactions on Power Delivery*, vol. 26, no. 1, pp. 307–315, Jan 2011.

[6] A. B. Shitole, H. M. Suryawanshi, S. Sathyan, and M. M. Renge, "*Adaptive notch filter based synchronization technique for integration of distributed generation systems to utility grid*," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, Oct 2014, pp. 5457–5461.

[7] G. Yin, L. Guo, and X. Li, "*An amplitude adaptive notch filter for grid signal processing*," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2638–2641, June 2013.

[8] A. B. Shitole, H. M. Suryawanshi, and S. Sathyan, "*Comparative evaluation of synchronization techniques for grid interconnection of renewable energy sources*," in *Industrial Electronics Society, IECON 2015 - 41st Annual Conference of the IEEE*, Nov 2015, pp. 001 436–001 441.

[9] A. Shitole, H. M. Suryawanshi, G. Talapur, s. sathyan, M. Ballal, V. B. Borghate, M. Ramteke, and M. Chaudhari, "Grid interfaced distributed generation system with modified current control loop using adaptive synchronization technique," *IEEE Transactions on Industrial Informatics*, vol. PP, no. 99, pp. 1–1, 2017.

[10] Mahtab Alam, Mr. Jitendra Kumar Garg,"*Comparative study of different topologies of five level inverter for harmonics reduction*",International journal of Advanced research in science and engineering,vol.no.4,Issue.07,July 2015.

First Author Dr.B.Gopinath, M.E.,Ph.D.,Associate Professor, Department of EEE.

Second Author Mr.M.Kalyanasundaram, M.E.,(Ph.D**).,** Assistant Professor, Department of EEE.

Third Author V.Karthika,PG student, Department of EEE.

Fourth Author M.Pradeepa,PG student, Department of EEE.