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Study of Switched Inductor Based Z-Source Cascaded H-Bridge Multilevel Inverter

P. Satheesh Kumar, Dr. S. P. Natarajan, Dr. Alamelu Nachiappan, Dr. B. Shanthi

***Abstract*— This paper proposes a Switched Inductor-Z-Source Cascaded H-Bridge Multilevel Inverter (SL-ZS-CHB-MLI). This proposed topology has wide applications in ac- ac, dc- ac, dc- dc, dc- ac power conversion. This topology is made up of numerous basic units. The number of basic unit required is based on the formula (n-1)/2, where n is the number of levels. Each basic unit in the proposed SL-ZS-CHB-MLI topology are developed by a Z-Source (ZS) network comprising switched inductor cells, and a H-Bridge cell. The proposed topology has high output voltage boosting capability due to the presence of switched inductor cells, which further reduces ripple contents in the input current. It is also having the advantage of lower voltage stress across capacitors. The proposed topology exhibits high output voltage boosting capability with lower THD. The principle of operation of shoot through and non-shoot through states of the SL-ZS-CHB-MLI is elucidated in detail with equivalent circuit diagrams. Capacitor voltages for each basic unit in the 11-level proposed topology have been presented. The Harmonic analysis of the proposed topology for 5, 7, 9 and 11 level output voltages is presented with simulated results obtained from MATLAB software.**

***Index Terms*— Z- Source network, Switched inductor, CHB-Multilevel Inverter, Simple boost inductor.**

I. INTRODUCTION

In modern research works, multilevel inverter has attracted extensive attention. High-power industrial applications requiring good quality output voltage. Multilevel inverters produce required output voltage from multiple DC voltage sources from renewable energy sources such as PV panel or windmill. The three topologies of multilevel inverters has been utilized in practice such as diode clamped, flying capacitor and cascaded H-bridge inverters [1-2]. The CHB inverter has more advantages than the other two topologies such as lower number of switching components in its configuration for the same number of levels [3-5]. Also, in modern days, numerous Z-source inverter (ZSI) topologies have been developed in recent research works [6–17]. The ZSIs facilitates a single-stage power conversion with buck and boost functionalities. In ZSIs, switching devices in a same leg can be turned on at the same time, which is not possible in traditional voltage source inverters. This property of the ZSIs avoids the dead time, increases the reliability and lowers the output voltage distortion.

The impedance-source networks in the ZSIs are extensively used to provide boost ability. The ZSI has tremendous applications in grid connected renewable energy sources. Despite of its advantages, the ZSI topology has few drawbacks, which includes high voltage stress across the capacitors and power switches, high inrush current, ripples and lower boost factor. A new concept of switched inductor (SL) technique has been introduced in the conventional ZSI to overcome aforementioned disadvantages and to improve the boost factor. The switched inductor Z-source inverter (SL-ZSI) overcomes the boost limitations of the conventional ZSI with size reduction and high power density. Also, the limitations allied with the ZSI such as high voltage stress on capacitors, discontinuous input current, and no common ground point between the CHB inverter and dc-source can be tackled with the development of the SL-ZSI inverters. The switched inductor increases the boost gain for the same shoot through duty ratio as compared with the traditional ZSI. The switched inductor permits the operation of the proposed topology at higher modulation index, thus minimizing the stress over the switching components. This paper proposes a Z-Source Cascaded H-Bridge Multilevel Inverter with Switched Inductor (SL-ZS-CHB-MLI), which combines the advantages of CHB multilevel inverter and switched inductor ZSI. Capacitor voltages for each unit in the 11-level proposed topology have been presented. Harmonic analysis of the proposed SL-ZS-CHB-MLI topology for 5, 7, 9 and 11 level output voltages has been presented. The proposed SL-ZS-CHB-MLI topology has lower THD and higher voltage boosting capability with improved output voltage as compared with traditional inverters. In the proposed topology, the 11 level output voltage exposes lower THD when compared with the other output voltage levels with reference to the simulation results.

The SL-ZS-CHB-MLI topology is explained in section II. The PWM control of the proposed SL-ZS-CHB-MLI is given in section III. The simulation results are presented in section IV, which depicts various output voltages with THD. Finally the conclusion is given in section V.

II. SWITCHED INDUCTOR Z-SOURCE CASCADED H-BRIDGE MULTILEVEL INVERTER TOPOLOGY

This proposed topology has wide difference from the view of existing structures .It has got the initial solution for the conflicts caused by M and D, for the high power quality and high boost inversion ability. This topology achieves the great increase in the boost factor from 1/(1-2D) to (1+D) / (1-3D)

The proposed topology SL-ZS-CHB-MLI is as shown in Fig.1.The figure 1 presents for seven levels. Further by adding two more modules, in the existing circuit, 11 level

P. Satheesh Kumar, Department of Electrical and Electronics Engineering, Mailam Engineering College, India,
Dr. S. P. Natarajan, Professor & Head (Retd), Department of Instrumentation Engineering, Annamalai University, India,
Dr. Alamelu Nachiappan, Professor & Head, Department of Electrical and Electronics Engineering, Pondicherry Engineering College, India,
Dr. B. Shanthi, Professor, Centralized Instrumentation and Service Laboratory, Annamalai University, India,

topology can be obtained. Seven level topology consists of three Z -source modules connected to Three H Bridge. Three H Bridge are cascaded among each other as shown in Fig.1. For further, circuit explanation purpose, one basic Z-source unit connected with one H bridge is considered. Each basic Z-source unit consists of one Voltage source, one input diode D_{in1}, two capacitors (C_1 & C_2,) connected in X shape and two switched inductor cells (top cell and bottom cell), one at the top of the Z source module and the other at the bottom of the Z source module.

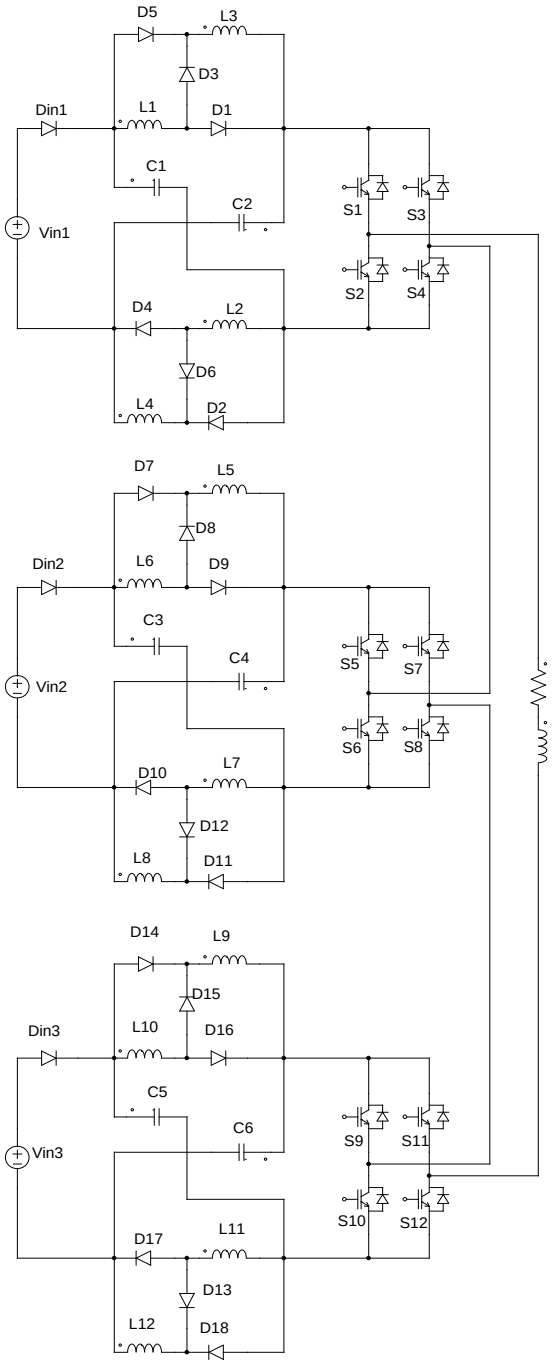

Fig.1.Circuit Diagram of the proposed Topology SL Z Source CHB MLI

Each Switched Inductor cell has symmetric structures and consists of three diodes and two inductors. The top switched inductor cell consists of L_1-D_1-D_5-D_3-L_3 arrangement as shown in Fig.1.The bottom switched inductor cell consists of L_2-D_4-L_4-D_6-D_2 arrangement as shown in Fig.1.Depending upon the switching action of the main circuit, there are two functions that each of the Switched inductor cells performs; They are 1) both the top cell and bottom cell are used to store energy and 2) both the top cell and bottom cell transfer energy from capacitors to the circuits. More or less the operation of the proposed topology is similar the classical Z source inverter from the view of switching states of the main circuit. Shoot Through mode and non-Shoot through mode are the two operating modes of this topology. The boosting function is done during shoot through mode.

A. *Shoot Through mode*

The circuit of the proposed topology in ST mode is shown in Fig. 2(b). In this, the input diode ($D_{in\,1}$) is turned off. The diodes D_3 and D_6 are also turned off but the diodes D_1 and D_5 from top cell and *D2* and *D4* from bottom cell are conducted. The inductances L_1, L_3 (top cell) and L_2, L_4 (bottom cell) are charged by Capacitors C_1 and C_2 respectively.

B. *Non-Shoot Through Mode*

The circuit of the proposed topology in ST mode is shown in Fig. 2(a).In this the input diode D_{in} 1 is turned ON. The diodes D_3 and D_6 are turned on but the diodes D_1 and D_5 from top cell and D_2 and D_4 from bottom cell are in of condition. Therefore the inductances L1 and L3 (top cell) are connected in series and delivers energy to the main circuit. The inductances L2 and L4 (bottom cell) are connected in series and delivers its energy to the main circuit. At this same duration, the capacitors C_1 is charged through the bottom cell and the capacitor C_2 is charged through the top cell from the input voltage source. Before this state starts, these two capacitors have delivered its stored energy to the inductors during shoot through state.

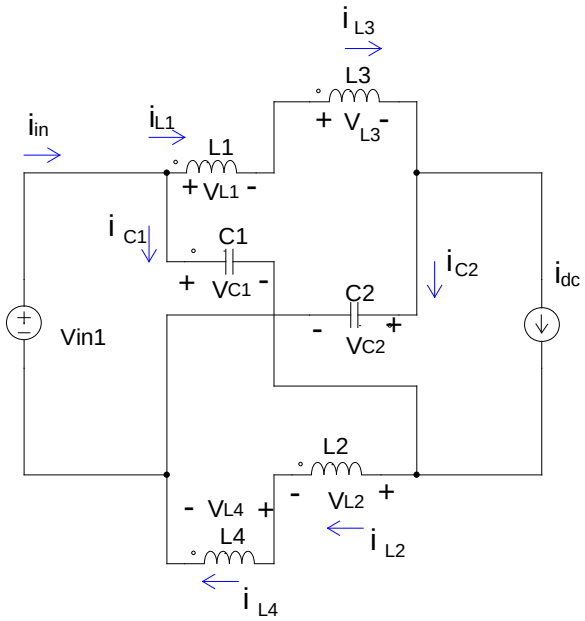

Fig. 2 (a). Non shoot-through state.

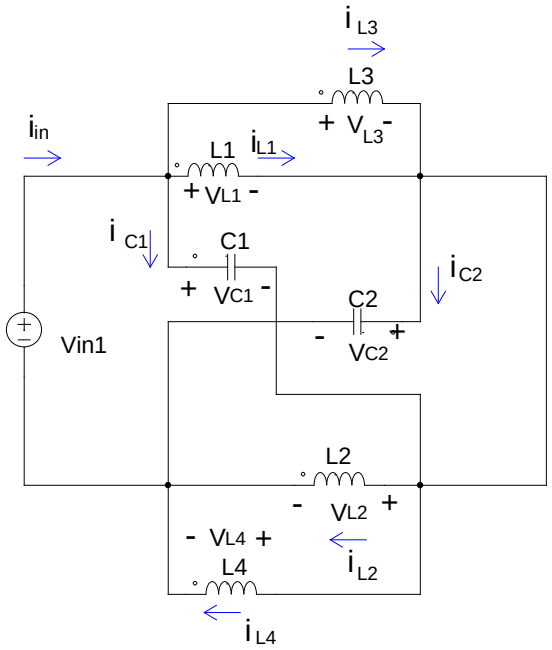

Fig.2(b). Shoot-through state.

III. PWM TECHNIQUE FOR THE PROPOSED SL-ZS-CHB-MLI

The modulation technique for this topology is described below. This topology has shoot through mode of operation, which the traditional inverters do not posses. Therefore some modifications are needed to be done in the traditional PWM technique, to consider shoot through state. In the existing PWM technique, an additional constant line, called shoot through line is used. Based on the magnitude of the shoot through line, there are three types of modulation strategies available. They are 1. Simple boost control. 2. Maximum boost control and 3.maximum constant boost control. Simple boost control technique is employed in this proposed topology.

A. Simple Boost Control

The reference wave is the sinusoidal waves. The carrier wave is the high frequency triangular wave. The shoot through state is realized by two straight lines. The magnitude of this two straight line must be greater than or equal to the reference wave. Here it is three phase sine wave with a phase difference of 120 degrees.

The shoot through mode is affected, whenever the triangular carrier signal is greater than the positive straight line or lowers than the negative straight line.

The corresponding switches in the upper limbs are switched on, during the period, when the amplitude of the sine wave is greater than the triangular carrier wave. The lower limb devices have the complement operation.

$$V_{C2} = \frac{1-D_{sh}}{1-3D_{sh}} V_{in} \quad (1)$$

$$V_{DC} = V_{C1} + V_{C2} = \frac{1+D_{sh}}{1-3D_{sh}} V_{in} = BV_{in} \quad (2)$$

$$V_o = M \cdot B \cdot \frac{V_{dc}}{2} \quad (3)$$

$$D_{sh} = \frac{T_{sh}}{T} = 1 - M \quad (4)$$

$$B = \frac{1+D_{sh}}{1-3D_{sh}} \quad (5)$$

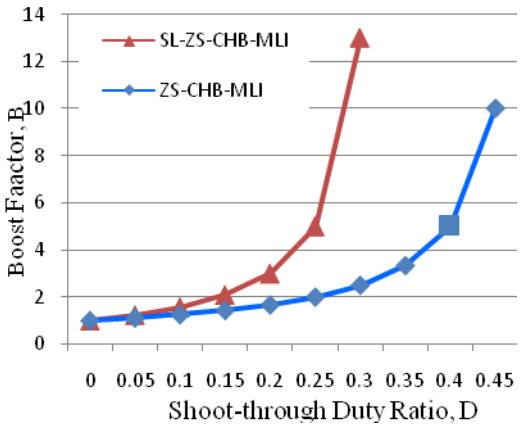

Fig.3 (a) Comparison between ZS-CHB-MLI and proposed topology for boost factor vs duty ratio

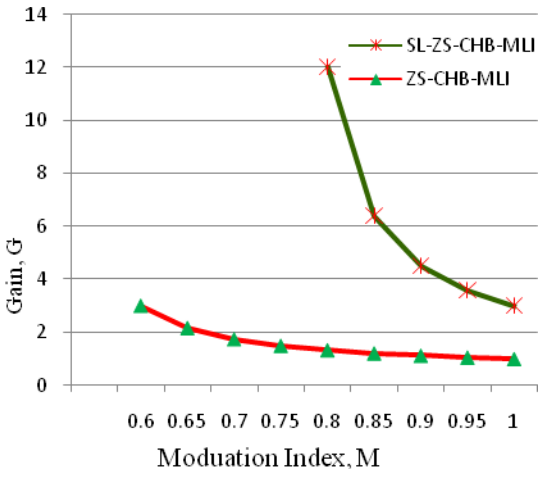

Fig.3 (b) Comparison between ZS-CHB-MLI and proposed topology for Gain Vs Modulation Index

The above fig 3(a) shows the proposed topology has better boost factor on comparing with the Z source CHB –MLI. The fig 3(b) shows that the proposed topology has better gain on comparing with the Source CHB –MLI. Observation from the graph, explains that, very low voltage boosting is happening at M=1, whereas when M<1, gradually voltage boosting becomes stronger than that of ZS-CHB-MLI .It is also noted that for any given gain, a higher modulation index is available in the proposed inverter which justifies improved performance.

IV. SIMULATION RESULTS

To analyze the performance of the proposed SL-ZS-CHB-MLI, the following simulation parameters are selected. L_1=L_2=L_3=L_4= 2mH. $C_1$and C_2 =2000µf, the

switching frequency is 10 kHz; the input was 100Vdc for each module. Simple boost control is used. The simulation is done for 5 level, 7 level 9 level and 11 level circuits. The 11 level circuits have five modules or basic unit. Each module has two capacitor whose voltages are V_{C1} and V_{C2}.The capacitor voltages of each module is shown in graph from Fig 4.1 to Fig 4.10.

The output voltage for the 11 level circuits which has better output voltage is shown in the Fig 5.1 .The DC link voltage for the 11 level is shown in the Fig. 5.2. The THD spectrum of 5 levels is shown in the Fig 5.3, the 7 level is shown in the Fig 5.4. The 9 level is shown in the Fig 5.5 and 11 levels is shown in the Fig 5.6.

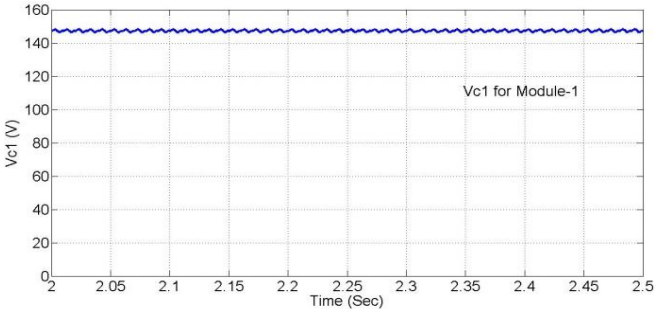

Fig 4.1 Capacitor C_1 Value for module 1 of 11 level inverter

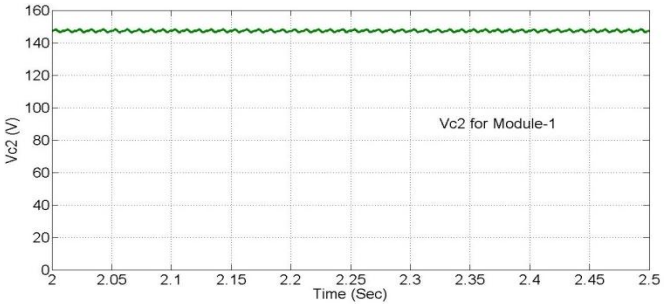

Fig 4.2 Capacitor C_2 Value for module 1 of 11 level inverter

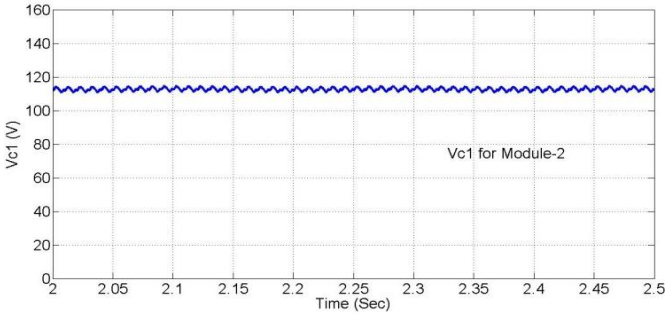

Fig 4.3 Capacitor C_1 Value for module 2 of 11 level inverter

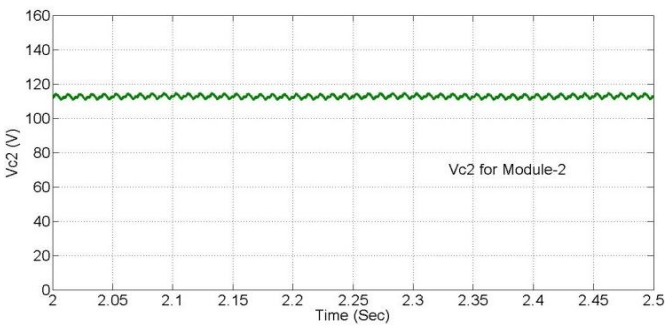

Fig 4.4 Capacitor C_2 Value for module 2 of 11 level inverter

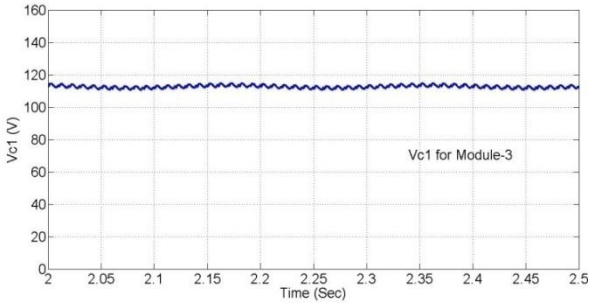

Fig 4.5 Capacitor C_1 Value for module 3 of 11 level inverter

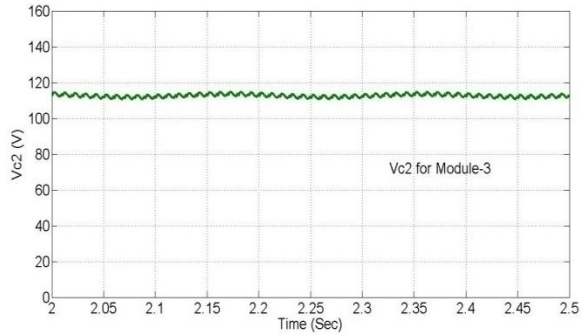

Fig 4.6 Capacitor C_2 Value for module 3 of 11 level inverter

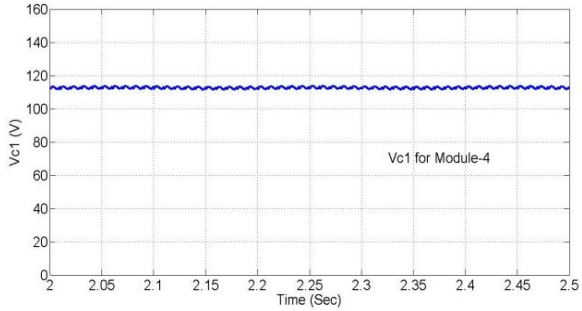

Fig 4.7 Capacitor C_1 Value for module 4 of 11 level inverter

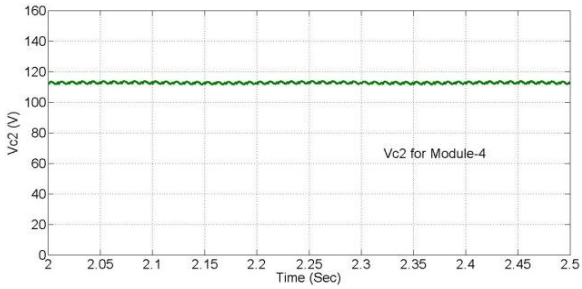

Fig 4.8 Capacitor C_2 Value for module 4 of 11 level inverter

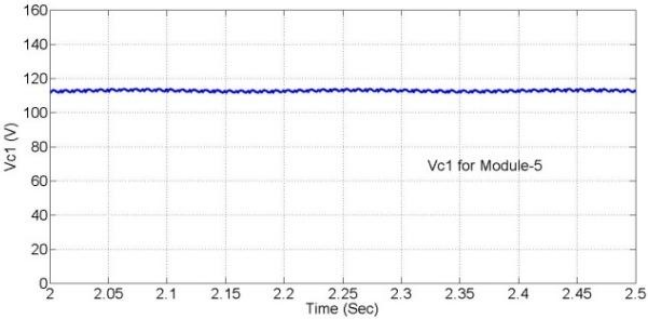

Fig 4.9 Capacitor C_1 Value for module 5 of 11 level inverter

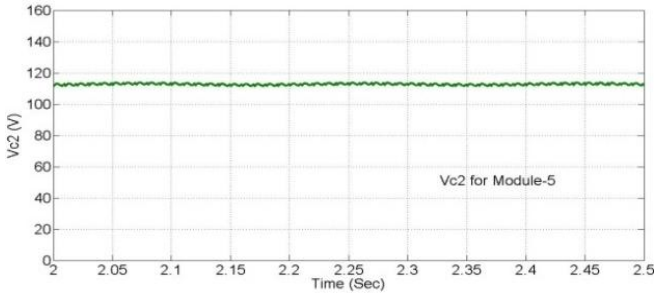

Fig 4.10 Capacitor C_2 Value for module 5of 11 level inverter

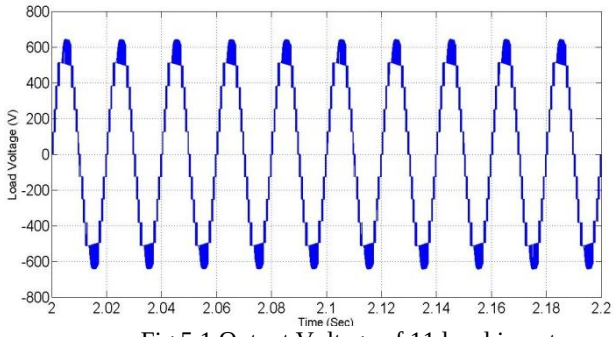

Fig 5.1 Output Voltage of 11 level inverter

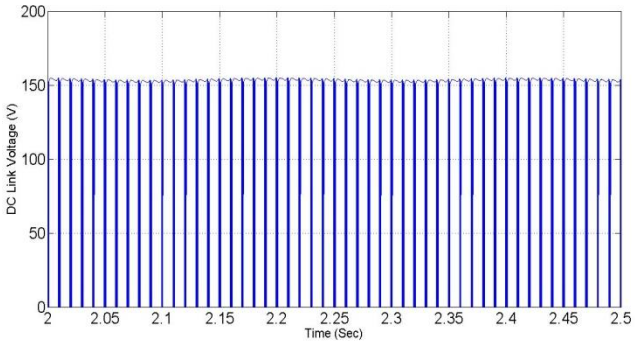

Fig 5.2 DC Link Voltage of 11 levels SL-ZS-CHB-MLI

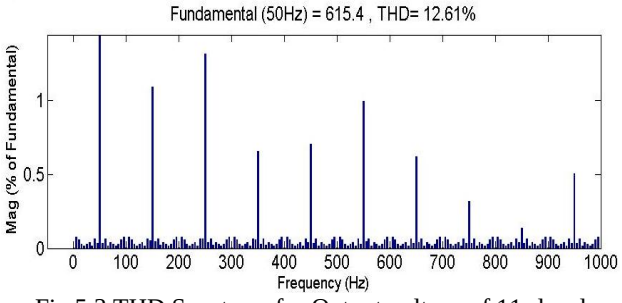

Fig.5.3 THD Spectrum for Output voltage of 11- level SL-ZS-CHB MLI

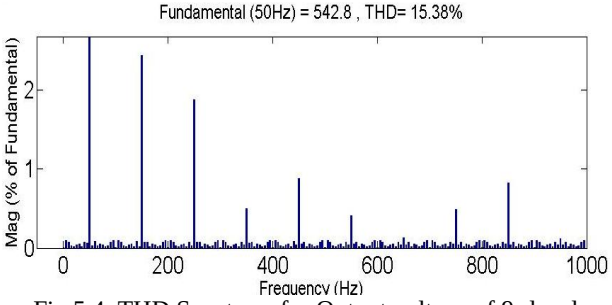

Fig.5.4. THD Spectrum for Output voltage of 9- level SL-ZS-CHB MLI

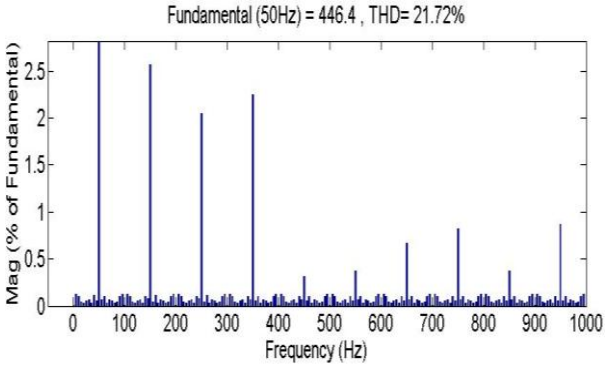

Fig 5.5. THD Spectrum for Output voltage of 7- level SL-qZS-CHB MLI

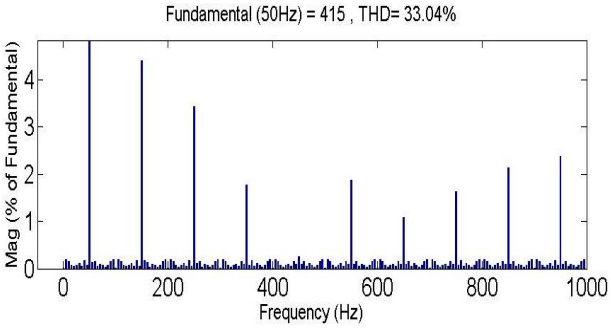

Fig 5.6 THD Spectrum for Output voltage of 5- level SL-ZS-CHB MLI

The increased boost factor and the gain provides the better performances for various level as given in the below table.1

Table I.Comparison between 5level vs 7 level vs 9 level vs 11 level

No.of Output Voltage levels	5	7	9	11
Input Voltage (V)	200	300	400	500
Output Voltage (V)	415	446.4	542.8	615.4
THD in Percentage	33.04	21.72	15.38	12.61

V. Conclusion

This paper proposed an SL-ZS-CHB-MLI with extended boost capability. The performance analysis of the proposed topology in terms of THD for different output voltage levels is presented with the simulated results using MATLAB. The output voltage and THD for 5,7,9 and 11 levels is presented in the comparison table 1.In this paper, the simulation result assures reduced THD for the eleven level output voltage when compared with 5, 7 and 9 level output voltage waveforms of the SL-ZS-CHB-MLI.

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Satheesh Kumar Packirisamy was born in 1979 and received the B.E. degree in the year 2001from the University of Madras and M.E .degree in the year 2004 from the Annamalai University and currently pursuing Ph.D. degree in the Annamalai University, He is having 13 years of experience. He is currently working as Associate Professor in the Department of Electrical and Electronics Engineering at Mailam Engineering College, Mailam, Tamilnadu, India. His research interests include Power Electronics and Multilevel Inverters. He is a life member of Indian Society for Technical Education.

Dr. S. P. Natarajan was born in 1955 in Chidambaram. He has obtained B.E (Electrical and Electronics) and M.E (Power systems) degrees in 1978 and 1984 respectively from Annamalai University securing distinction and then PhD in Power Electronics from Anna University, Chennai in 2003. He is currently Professor and Head of Instrumentation Engineering Department at Annamalai University (Retd) where he has put in 31 years of service. He produced nine PhDs and presently guiding nine Ph.D Scholars and so far guided eighty M.E students. His research papers 105 have been presented in various/IEEE international/national conferences in Mexico, Virginia, Hong Kong, Malaysia, India, Singapore and Korea. He has 15 publications in national journals and 142 in international journals. His research interests are in modeling and control of DC-DC converters and multiple connected power electronic converters.

Dr. Alamelu Nachiappan received the B.E. (Electrical and Instrumentation) degree in the year 1984 and M.E. degree in the 1988 from the Annamalai University and then obtained her Ph.D. from the Pondicherry University in the year 2007. She is having 28 years of experience. She is presently a Professor and Head in the Department of Electrical and Electronics Engineering at Pondicherry Engineering College, Pondicherry. She has published and/or presented more than 81 papers in International / National journals and conferences. Her research interests include digital signal processing techniques and power control. She is a Fellow of Institution of Engineers (India).

Dr.B.Shanthi was born in 1970 in Chidambaram. She has obtained B.E (Electronics and Instrumentation) and M.Tech (Instrument Technology) from Annamalai University and Indian Institute of Science, Bangalore in 1991 and 1998 respectively. She obtained her Ph.D. in Power Electronics from Annamalai University in 2009. She is presently a Professor in Central Instrumentation Service Laboratory of Annamalai University where she has put in a total service of 24 years since 1992. Her research papers (65) have been presented in various international /national seminars/conferences. She has 47 publications in national journals and 61 in international journals. Her areas of interest are: modeling, simulation and intelligent control for MLI and Z-source inverters.